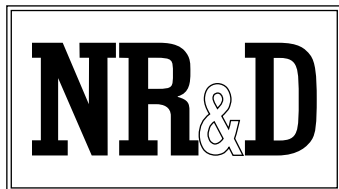


SPXM

Installation and Programming Manual

This Manual describes the SPXM Seriplex Master, its uses and set up. It also describes the use of the SPXM configuration software.

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Introduction

The Niobrara SPXM allows a Sy/Max PLC to interact with I/O points and devices via the Seriplex Sensor/Actuator bus. Seriplex is an efficient, inexpensive, deterministic bus interconnecting up to 255 I/O points or 240 16 bit words using a four wire cable. The SPXM supports both Seriplex Mode 1 (peer-to-peer) and Mode 2 (host-controlled) configurations.

The SPXM connects to the Seriplex cable through a front-mounted, male 9 pin D-subminiature connector. All Seriplex circuits are optically isolated from PLC electronics.

An external power supply is required. Only one host interface (such as SPXM) at a time should be connected to the Seriplex bus and no clock module should be connected when an SPXM is used. The SPXM supplies the Seriplex clock and sources pull-up current to the Seriplex data line.

The SPXM interfaces to the Sy/Max PLC through rack-addressed registers. The first of these registers configures the SPXM and the others are mapped to Seriplex peripherals. The layout of the I/O registers depends on the configuration register. The SPXM supports any length of Seriplex bus up to 256 bits in multiples of 16. The SPXM supports multiplexing of 4, 8, 12, or 16 channels deep by up to 240 bits wide in multiples of 16 bits. Multiplexed words must be positioned on 16 bit boundaries and must occupy the highest numbered bits of the configured Seriplex address space.

The actual value placed in register 1 may easily be determined with the assistance of the SPXMSW.EXE program. This MS-DOS program provides a convenient interface for determining the configuration of the SPXM. This software is provided free of charge with the SPXM.

Specifications

Module Specifications

Mounting Requirements

One register slot of a Square D Class 8030 Type CRK, DRK, GRK, HRK, or RRK I/O.

Current Draw on SY/MAX power supply

500 mA

Operating Temperature

0 to 60 degrees C operating. -40 to 80 degrees C storage.

Humidity Rating

up to 90% noncondensing

Pressure Altitude

-200 to +10,000 feet MSL

Seriplex Communication Port

9 pin male D-connector. Variable frequency (16, 32, 64, 100) Kbaud Seriplex protocol. Supports Mode 1 and Mode 2 and Multiplexed analog I/O.

Indicator lights

4 LEDs: Green Power, Green Run, Red Undervoltage, and Red Fault.

Physical Dimensions

Single width module.

Wt: 2.5 lb.

W: 1.5 in.

H: 12.8 in.

D: 6.6 in.

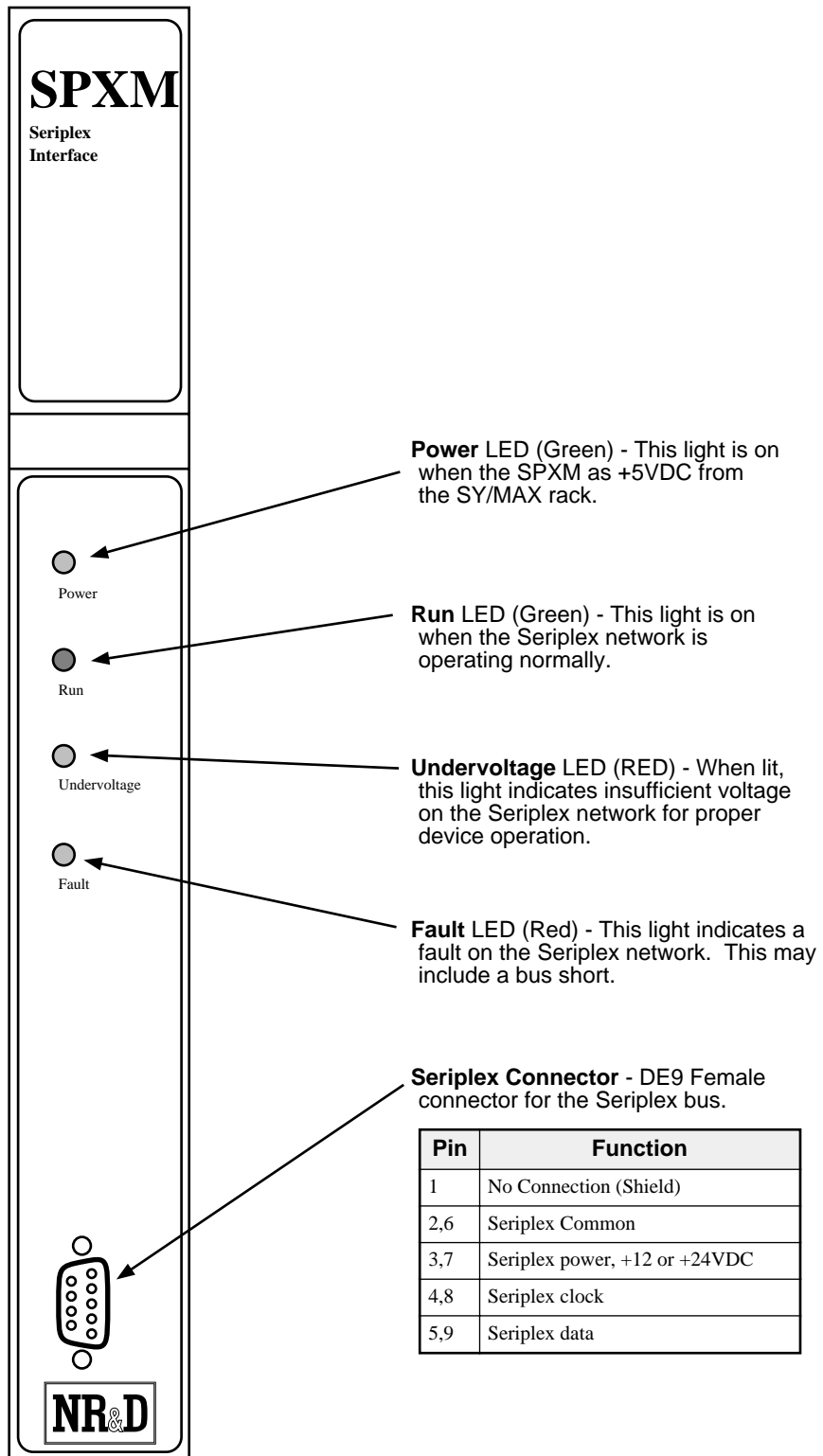


Figure 1-1 SPXM Front Panel

Warning

Do NOT install or remove the SPXM with power applied to the Rack. Turn OFF power at the power supply. Damage to the equipment may occur if the power is on during installation.

Module Installation

- 1 Remove power from the rack.
- 2 Mount the SPXM in an available slot in the register rack. Secure the screw at the bottom of the module.
- 3 Apply power to the rack. The green power light should illuminate and remain lit. Since the Seriplex network is not attached, the red Undervoltage light should also be on.

NOTE: If the slot that the SPXM occupies has been rack addressed by the PLC and the first register that is assigned to the SPXM contains a valid SPXM configuration value, the PLC will likely display an I/O Error and go into Halt. This is an example of the BUS error feature of the SPXM. When a PLC BUS error occurs, Register 8175 in the PLC will display the decimal number 19000 + First register rack addressed to the module. For example, the SPXM is in a slot rack addressed from 640 to 675. When a bus error occurs, the decimal value 19640 will appear in PLC register 8175.

SPXMSW Software Installation

This MS-DOS compatible program runs on an IBM compatible personal computer. The software is distributed on a 3.5" 1.44M floppy and is compressed using an industry standard .ZIP format. For automatic installation perform the following steps.

- 1 Insert the floppy into a drive and run the INSTALL program from that drive.
- 2 Enter the floppy drive name that contains the distribution disk.
- 3 Select SPXMSW from the list of softwares to install.

- 4 Enter a directory name to install the SPXMSW software. It is recommended that a directory SPXM be used for the installation on your hard drive.
- 5 Once INSTALL is finished copying and expanding the files, exit by pressing the ESC key until the DOS prompt is reached.
- 6 Change to the SPXM directory and perform a directory with the following commands:

```
C:
CD \SPXM
DIR
```

Table 2-1 lists the files that should appear in the directory. These files are described in Chapter 4 on page 17.

Table 2-1 SPXM Software List

File Name	Description
SPXMSW.EXE	SPXM Configuration Software.
SPXM.ICO	Icon for SPXMSW for Windows.



Figure 2-1 SPXMSW Screen

Seriplex installation

The SPXM connects to the Seriplex network using its 9 pin port. The pinout of this connector and the suggested wire colors for the Seriplex network cable is shown in Table 2-2.

Table 2-2 SPXM Seriplex Connector

Pin	Function	Suggested Wire Color
1	No Connection (Shield)	Bare
2,6	Seriplex Common	Black
3,7	Seriplex power, +12 or +24VDC	Red
4,8	Seriplex clock	Green
5,9	Seriplex data	White

Power Supply

An isolated 12VDC. power supply is required for the Seriplex network. Square D recommends the use a source with line regulation of +/- .05% for a 10% AC line change. With a 50% load change, the voltage output should change no more than +/- .05% and the output ripple should be 5.0mV PK-PK

maximum. It is recommended that the current capacity be rated at 1.2 times the total load current of the network. Also, long cable runs may result in voltage drop, so multiple power supplies may need to be included in the network.

Clock Module

The SPXM provides the clock signal for the Seriplex network in Mode 1 and Mode 2. **The external clock module is not required and should NOT be used.**

Seriplex Overview

The Niobrara SPXM allows a Sy/Max PLC to interact with I/O points and devices via the Seriplex Sensor/Actuator bus. Seriplex is an efficient, inexpensive, deterministic bus interconnecting up to 255 I/O points or 240 16 bit words using a four wire cable. The SPXM supports both Seriplex Mode 1 (peer-to-peer) and Mode 2 (host-controlled) configurations.

The SPXM connects to the Seriplex cable through a front-mounted, male 9 pin D-subminiature connector. All Seriplex circuits are optically isolated from PLC electronics. The pinout of the Seriplex connector is as follows:

- 1 - No internal connection, Seriplex shield may be connected here
- 2,6 - Seriplex common
- 3,7 - Seriplex power,+12 or +24 volts
- 4,8 - Seriplex clock
- 5,9 - Seriplex data

An external power supply is required. Only one host interface (such as SPXM) at a time should be connected to the Seriplex bus and no clock module should be connected when an SPXM is used. The SPXM supplies the Seriplex clock and sources pull-up current to the Seriplex data line.

The SPXM interfaces to the Sy/Max PLC through rack-addressed registers. The first of these registers configures the SPXM and the others are mapped to Seriplex peripherals. The layout of the I/O registers depends on the configuration register. The SPXM supports any length of Seriplex bus up to 256 bits in multiples of 16. The SPXM supports multiplexing of 4, 8, 12, or 16 channels deep by up to 240 bits wide in multiples of 16 bits. Multiplexed words must be positioned on 16 bit boundaries and must occupy the highest numbered bits of the configured Seriplex address space.

Seriplex bits are numbered 0 through 255. Sy/Max register bits are numbered 1 through 16. Keep this in mind when reading the following discussion. For instance, the Sy/Max rack-addressed input SPXM register 2 bit 11 corresponds to Seriplex bit

address 10. While the bit mapping could have been aligned, especially since Seriplex bit 0 is unused, this would lead to inconvenience in processing byte and word data in Seriplex modules assigned to bit addresses that are multiples of 8 or 16.

Rack-addressed register 1 of the SPXM is the configuration register and is divided into eight fields as follows. Within each field, the highest numbered bit is the most significant. The status field of the register is A000 hex indicating a PLC output. After September, 1995, bits 9 and 10 of the status field are set to indicate error conditions. (These are PLC bits 25 and 26.)

Bits	Function	Values
-----	-----	-----
4,3,2,1	Seriplex bus length including multiplexed words, mux channel bits, and unused bit 0.	0000 = 16 bits 0001 = 32 bits 0010 = 48 bits 0011 = 64 bits 0100 = 80 bits 0101 = 96 bits 0110 = 112 bits 0111 = 128 bits 1000 = 144 bits 1001 = 160 bits 1010 = 176 bits 1011 = 192 bits 1100 = 208 bits 1101 = 224 bits 1110 = 240 bits 1111 = 256 bits
8,7,6,5	Number of multiplexed words. Must be less than or equal to bus length.	0000 = no multiplex 0001 = 1 word 0010 = 2 words 0011 = 3 words 0100 = 4 words 0101 = 5 words 0110 = 6 words 0111 = 7 words 1000 = 8 words 1001 = 9 words 1010 = 10 words 1011 = 11 words 1100 = 12 words 1101 = 13 words 1110 = 14 words 1111 = 15 words
10,9	Clock rate	00 = 16 KHz 01 = 32 KHz 10 = 64 KHz 11 = 100 KHz

12,11	Multiplex depth	00 = 4 channels 01 = 8 channels 10 = 12 channels 11 = 16 channels
13	Seriplex Mode	0 = Mode 2, host controlled 1 = Mode 1, peer-to-peer
14	Error Inhibit	0 = Halt PLC on fault. 1 = No bus error on fault. Monitor status bits of register 1 for error identification.
15	Reserved	0
16	Run control	0 = continuous long reset 1 = run

Register 1 status bits (PLC bit number)

9 (25)	Undervoltage	0 = Proper voltage. (UVOLT light off) 1 = Undervoltage condition. (light on)
10 (26)	Other fault condition	0 = No other fault. (FAULT light off) 1 = Other fault condition (light on)

In mode 1, the 64 KHz speed setting will actually clock the bus at 64.5 KHz.

The layout of the remaining registers of the SPXM depends on the configuration. Following the configuration register, there is one input word for each non-multiplexed word (or fraction) of I/O. Following the inputs are one output word for each non-multiplexed word of I/O. In mode 2, the input register indicates the state of input points on the bus (even clock cycles) and the output register determines the driven state of output modules (odd clock cycles). In mode 1, the input registers reflect the state of the Seriplex bits whether driven by modules on the bus or by the SPXM and the output registers are wire-ored with field inputs occupying the same addresses.

Following the non-multiplexed registers are registers for the configured number of multiplexed words. First are the input registers for all multiplexed words, following are the output registers for all multiplexed words. The behavior of these bits is similar to the non-multiplexed bits described above, including mode 1 and mode 2 operations, but the scan rate is slower, being divided between the multiplexed channels. Within the banks of input and output registers, all of the channels of the first module appear followed by all of the channels of each additional module.

When multiplexing is enabled, the SPXM drives the Seriplex multiplex channel bits from an internal counter and ignores the state of the associated output register bits (bits 2 through 5 of the first non-multiplexed output register). In mode 1, the channel bits may be examined in bits 2 through 5 of SPXM register 2. In mode 2, these bits are available for Seriplex inputs.

Seriplex bit zero is unavailable for I/O but is mapped to the PLC rack. The PLC output bit which corresponds to Seriplex bit 0 is ignored and the associated input bit (SPXM register 2 bit 1) always reads as zero.

If the PLC is set to disable outputs or is halted, all Seriplex outputs will be set to zero (i.e. Seriplex data line allowed to float). In the case of a Seriplex fault detected by the SPXM, a bus error will be posted to the PLC and one of the red LED indicators on the front of the SPXM will light. The SPXM can detect undervoltage, clock shorted low, clock shorted high, data shorted low, data shorted high, and external clock source error conditions. Please note that, in mode 1, output disable from the PLC will not turn off any outputs driven directly by Seriplex inputs. Configuration register bit 16 can be cleared to set all outputs to their shelf state.

Configuration of the SPXM is fully dynamic. It is not even necessary to halt the Seriplex bus before modifying bits 1 through 13 of the configuration register. Of course, if the new configuration doesn't match the hardware, you could halt the PLC with an error. For example, driving mode 1 modules with a mode 2 host can result in a bus fault. There is one restriction to dynamic configuration with bit 16 set. If the new configuration consumes less rack space than the old one, any registers that were PLC inputs in the old configuration but are unused in the new configuration will not change to PLC outputs. If bit 16 is cleared either before, concurrently, or after writing the new configuration, all unused registers will be configured as PLC outputs.

Configuration Software SPXMSW

The SPXMSW software program is provided free of charge to SPXM users. This software is used to help configure the operation of the SPXM.

Data Entry Keys

Whenever data entry is allowed by the program, certain keys can be used to facilitate data entry. They are:

BACKSPACE	Move cursor left and remove character there
LEFT ARROW	Move cursor to the left one character
RIGHT ARROW	Move cursor to the right one character
DEL	Remove the character under the cursor
INS	Change between insert and overstrike modes of entry
HOME	Move cursor to the left edge of the field
END	Move cursor to the end of the data
Control-F	Move cursor right (Forward) one word
Control-R	Move cursor left (Reverse) one word
Control-D	Delete from the cursor to the end of the field
Control-U	Delete from cursor to the beginning of the field
Control-Y	Delete all characters in the field
ESC	Exit the field without modifying it
ENTER	Accept the contents of the field

When a field is opened for input, the cursor is positioned at the left side of the field. If data is already present in the field, typing any character other than those listed above will cause the field to be blanked allowing entry of new data without first deleting the old. If it is desired to retain the previous data for editing, make sure the first key you type is an editing key such as a left or right arrow.

Operation

The screen of SPXMSW is shown in Figure 4-1.



Figure 4-1 SPXMSW Screen

The cursor is used to move around the screen. The space bar, +, and - keys are used to change values. The object is to determine the exact configuration of the Seriplex network by setting all of the appropriate values. SPXMSW will display the appropriate values to load into register 1 for each configuration. SPXMSW will also provide the scan times for multiplexed and non-multiplexed scans of the Seriplex network.

The **ESC** key will allow the user to exit the program.

The **F1** key will perform a print screen.

The **F2** key will print a register map.

Entry Items

The following items are allowed to be modified. Note: certain values will interact with other values such as the number of multiplexed words will affect the bus size.

Seriplex Mode - This item allows the selection of the mode of operation on the Seriplex network. MODE 1 allows peer operation. MODE 2 allows the SPXM to act as the HOST of the network.

Seriplex bus size - This value sets the number of bits of data on the network. Choices include 16, 32, 48, 64, 80, 96, 112, 128, 144, 160, 176, 192, 208, 224, 240, and 256. This value may be set directly but is also calculated upon the number of multiplexed words.

Multiplexed words - Sets the number of multiplexed words on the Seriplex network. Values range from 0 through 15.

Multiplexed channels - This value sets the depth of the multiplexed registers. Available settings are 4, 8, 12, and 16.

Seriplex clock speed - This value determines the Seriplex network clock rate. Possible values are 16, 32, 64, and 100 kHz.

Rack address start - The Rack address start value is provided to allow the SPXMSW to print an accurate register map.

Displayed Items

The following items are display only and are calculated upon the setable items from above.

Rack address end - This value shows the last register in the PLC effected by the SPXM. This value is based upon the entered Rack address start value.

Run configuration - This is the numeric value that is to be loaded into the first register of the SPXM to configure the module to run with the selected parameters. This value is displayed in hexadecimal, signed decimal, and unsigned decimal. The user will most likely use the signed decimal value in a LET rung in the PLC ladder program to configure the module.

Reset configuration - This is the numeric value that is to be loaded into the first register of the SPXM to reset the module with the selected parameters. This value is displayed in hexadecimal, signed decimal, and unsigned decimal. The user will most likely use the signed decimal value in a LET rung in the PLC ladder program to configure the module.

Non-multiplexed scan time - This is the calculated scan time for the Seriplex network based upon the operating mode, the number of bits and the clock speed. This is the time between updates of the non-multiplexed I/O.

Multiplexed scan time - This is the calculated scan time for the multiplexed registers on the Seriplex network. It is most heavily influenced by the number of multiplexed channels.

Example configuration

Let us examine an imaginary Seriplex system including the SPXM, a power supply, ten Seriplex discrete I/O modules, and four sixteen bit analog I/O modules, each multiplexed across eight channels. The system will be configured in mode 2 for independent inputs and outputs under host control and will be clocked at 16KHz. The SPXM is located in a slot with a rack address starting at PLC register 400.

The discrete I/O modules occupy a total of 20 bits of non-multiplexed I/O comprising two bits (A and B) for each Seriplex module. Another four bits of non-multiplexed I/O is allocated for the multiplex channel address and one bit must be included for inaccessible Seriplex bit zero. Therefore, the Seriplex bus width must be at least 25 bits. The SPXM bus size must be programmed in multiples of 16 bits, so we configure 32 bits of non-multiplexed I/O. Sixty-four bits must be allocated for the four multiplexed modules. Therefore, the overall Seriplex bus size should be 32 + 64 or 96 bits and configuration register 1 bits 4,3,2, and 1 should be 0,1,0,1 respectively.

The multiplexed analog channels will occupy the last 64 bits of the Seriplex address space. In this example, bits 32 through 95. To configure four, 16 bit words of multiplex I/O, set bits 8,7,6, and 5 to 0,1,0,0 respectively.

The multiplex depth should be set to eight channels by programming configuration bits 12 and 11 to 0 and 1 respectively.

We will set the clock to 16 KHz by setting configuration bits 10 and 9 to zero.

Clearing configuration bit 13 selects Seriplex mode 2 and setting bit 16 instructs the SPXM to start scanning the bus.

The PLC ladder program should include a LET rung setting SPXM register 1 (PLC register 400) to 1000 0100 0100 0101 (8445 hex or -31,675 decimal).

The non-multiplexed I/O modules should be addressed at bits 5 through 24. The multiplexed modules should occupy bits 32 through 47, 48 through 63, 64 through 79, and 80 through 95.

The SPXM rack image will consist of 69 registers (PLC registers 400 - 468) organized as follows:

Seriplex SPXM Rack Address Map
=====

Seriplex operation in host controlled mode 2.
 Seriplex bus size 96 bits
 including 32 non-multiplexed bits and 4 multiplexed words.
 Bits 32 through 95 are multiplexed across 8 channels.
 Seriplex bits 1,2,3, and 4 are reserved for multiplex channel.
 Seriplex clock speed 16 kilohertz.

Set configuration to 0445 hex, 1093 decimal, or 1093 unsigned for RESET.
 Set configuration to 8445 hex, -31675 decimal, or 33861 unsigned for RUN.

Register	Direction	Seriplex Bits	Seriplex Channel
400	PLC Output	SPXM Configuration, set to -31675.	
401	PLC Input	0 through 15	
402	PLC Input	16 through 31	
403	PLC Output	0 through 15	
404	PLC Output	16 through 31	
405	PLC Input	32 through 47	1
406	PLC Input	32 through 47	2
407	PLC Input	32 through 47	3
408	PLC Input	32 through 47	4
409	PLC Input	32 through 47	5
410	PLC Input	32 through 47	6
411	PLC Input	32 through 47	7
412	PLC Input	32 through 47	8
413	PLC Input	48 through 63	1
414	PLC Input	48 through 63	2
415	PLC Input	48 through 63	3
416	PLC Input	48 through 63	4
417	PLC Input	48 through 63	5
418	PLC Input	48 through 63	6
419	PLC Input	48 through 63	7
420	PLC Input	48 through 63	8
421	PLC Input	64 through 79	1
422	PLC Input	64 through 79	2
423	PLC Input	64 through 79	3
424	PLC Input	64 through 79	4
425	PLC Input	64 through 79	5
426	PLC Input	64 through 79	6
427	PLC Input	64 through 79	7
428	PLC Input	64 through 79	8
429	PLC Input	80 through 95	1
Register	Direction	Seriplex Bits	Seriplex Channel
430	PLC Input	80 through 95	2
431	PLC Input	80 through 95	3
432	PLC Input	80 through 95	4
433	PLC Input	80 through 95	5
434	PLC Input	80 through 95	6
435	PLC Input	80 through 95	7
436	PLC Input	80 through 95	8
437	PLC Output	32 through 47	1
438	PLC Output	32 through 47	2

439	PLC Output	32 through	47	3
440	PLC Output	32 through	47	4
441	PLC Output	32 through	47	5
442	PLC Output	32 through	47	6
443	PLC Output	32 through	47	7
444	PLC Output	32 through	47	8
445	PLC Output	48 through	63	1
446	PLC Output	48 through	63	2
447	PLC Output	48 through	63	3
448	PLC Output	48 through	63	4
449	PLC Output	48 through	63	5
450	PLC Output	48 through	63	6
451	PLC Output	48 through	63	7
452	PLC Output	48 through	63	8
453	PLC Output	64 through	79	1
454	PLC Output	64 through	79	2
455	PLC Output	64 through	79	3
456	PLC Output	64 through	79	4
457	PLC Output	64 through	79	5
458	PLC Output	64 through	79	6
459	PLC Output	64 through	79	7
460	PLC Output	64 through	79	8
461	PLC Output	80 through	95	1
462	PLC Output	80 through	95	2
463	PLC Output	80 through	95	3
464	PLC Output	80 through	95	4
465	PLC Output	80 through	95	5
466	PLC Output	80 through	95	6
467	PLC Output	80 through	95	7
468	PLC Output	80 through	95	8

Unallocated but rack-addressed registers will be configured as PLC outputs and their contents ignored by the SPXM.

The Seriplex scan rate will be 16 KHz / (96 * 2 + 8) or about 12.5 milliseconds. The multiplexed channels will be updated at one eighth of this speed or every 100 milliseconds. A Sy/Max model 650 consumes about 40 microseconds of scan time per rack addressed register so rack-addressing the SPXM in this configuration will add about 2.8 milliseconds to the PLC scan time.

Figure 5-1 displays the SPXMSW screen with this example configuration.

```

SPXM SERIPLEX HOST ADAPTER
Niobeera R&D CONFIGURATION MENU 12May95

Seriplex mode HOST Mode 2
Seriplex bus size 96 bits
Multiplexed words 4
Multiplexed channels 8
Seriplex clock speed 16 kilohertz
Rack address start 000
Rack address end 468

SM Configuration 0445 Hex, -21475 Decimal, 33861 Assigned
SSEI Configuration 0445 Hex, 1093 Decimal, 1093 Assigned

Non-multiplex scan time 12.5 milliseconds
Multiplex scan time 100.0 milliseconds

Use up and down arrows to move highlight. Type + or - to change value.
Type F1 to print screen
Type F2 to print register map

For assistance, call Niobeera at (888)225-6723 or BSA (417)624-8718
Copyright (c) 1995 Niobeera R&D Corporation. All rights reserved.

```

Figure 5-1 SPXMSW Example screen

Connector Pinouts

Seriplex Port (DE9S with slide lock posts)

Pin	Function
1	No Internal Connection. May be used for Seriplex Shield
2,6	Seriplex Common
3,7	Seriplex power, +12 or +24VDC
4,8	Seriplex clock
5,9	Seriplex data

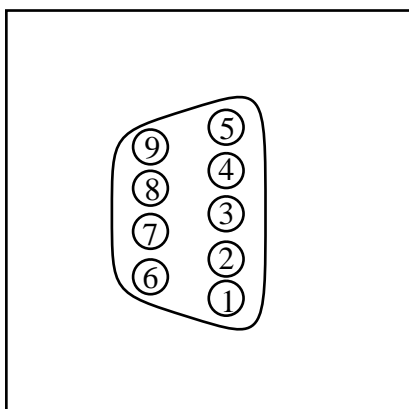


Figure 6-1 Seriplex Connector Pinout

Trouble Shooting

Undervoltage

When the voltage on the Seriplex network falls below the minimum working range, the red Undervoltage light comes on. If bit 14 of the first register assigned to the SPXM is not set, the SPXM will cause a bus fault on the PLC and cause the PLC to halt, and turn on the I/O error light on the PLC.

Undervoltages may occur due to a cable break between the SPXM and the Seriplex power module, a loss of power to the power module, a cable short somewhere on the network, or a faulty power module. A DC voltage meter is a handy tool for tracing power problems.

After the undervoltage problem is solved, the PLC must be halted, (with the key-switch or software) and then commanded to return to the RUN state to clear the I/O error.

When the Undervoltage light is on, the RUN light on the SPXM will be off. The Seriplex network will not run while a fault condition exists within the SPXM. All Seriplex devices will revert to their programmed default state.

If bit 14 of the first register of the SPXM is set, the PLC will not receive an I/O error. The SPXM will instead, turn on bit 9 of the status register for the first register in the module. The PLC may use this bit (bit 25) to control its ladder code operation.

Fault

In addition to the Undervoltage condition, the SPXM can detect the following:

- Clock shorted low
- Clock shorted high
- Data shorted low
- Data shorted high
- External clock active
- Running Mode 1 devices with a Mode 2 Host may sometimes generate a Fault. Especially at a high clock rate (100kHz).

If any of these situations occur, the red Fault light will be lit and if bit 14 of the first register assigned to the SPXM is clear the SPXM will cause a bus fault on the PLC. The PLC will then HALT and the red I/O error light will come on.

The SPXM will not give any indication to the type of fault that caused the system to stop. The user is required to check each of the data lines to determine if the problem is cable related.

When the Fault light is on, the RUN light on the SPXM will be off. The Seriplex network will not run while a fault condition exists within the SPXM. All Seriplex devices will revert to their programmed default state.

If bit 14 of the first register of the SPXM is set, the PLC will not receive an I/O error. The SPXM will instead, turn on bit 10 of the status register for the first register in the module. The PLC may use this bit (bit 26) to control its ladder code operation.

Appendix A

NR&D/Online BBS and Internet

Niobrara Research & Development is currently offering a Bulletin Board Service for its customers. This valuable customer service tool makes it easy to bring the user up to date on software revisions, firmware changes, product support news, and more.

This BBS operates on a 24 hour a day basis and is accessible from any personal computer equipped with a Hayes compatible modem. **NR&D/Online** will support communications from 300 to 9600 baud, at 8 data bits, NO parity, and 1 stop bit. Set your communications software for the baud rate of your modem, 8 data bits, NO parity, and 1 stop bit, then dial (417) 624-2028 to connect to **NR&D/Online**.

Once connected, you will find a message center, product bulletins, downloadable files and software, plus other news from the NR&D product support team.

Access and online time for **NR&D/Online** is free! You simply pay for your phone call.

For more information about **NR&D/Online** call Tom Fahrig at (800) 235-6723. He will take your information to allow you to log on to **NR&D/Online**.

Niobrara is also on the World Wide Web! Visit our home page at **<http://niobrara.com>** to see product information, cutsheets, application notes, and ftp current software releases.

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