QSPXM

Installation and Programming Manual

This Manual describes the QSPXM (Quantum Seriplex Master), its uses and set up.

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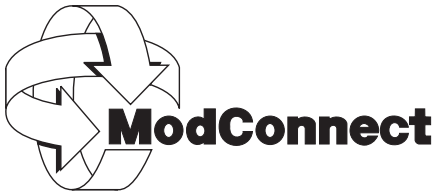

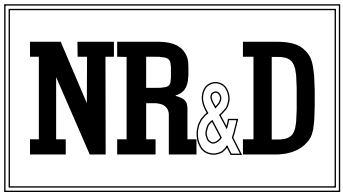

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Introduction

The Niobrara QSPXM allows a Modicon TSX Quantum Automation Series PLC to interact with I/O points and devices via the Seriplex Sensor/Actuator bus. Seriplex is an efficient, inexpensive, deterministic bus interconnecting up to 255 I/O points or 240 16-bit words using a four wire cable. The QSPXM supports both Seriplex Mode 1 (peer-to-peer) and Mode 2 (host-controlled) configurations.

The QSPXM contains Seriplex technology and conforms to the latest Seriplex standard. The QSPXM connects to the Seriplex cable through a front-mounted, male 9 pin D-subminiature connector. All Seriplex circuits are optically isolated from PLC electronics.

An external power supply is required. Only one host interface (such as QSPXM) at a time should be connected to the Seriplex bus and no clock module should be connected when the QSPXM is used. The QSPXM supplies the Seriplex clock and sources pull-up current to the Seriplex data line.

The QSPXM interfaces to the Quantum PLC as an I/O module and is thus permitted to be used in the Local (CPU rack), Remote (RIO), or Distributed (DIO) I/O racks[1]. The QSPXM is Traffic Copped as an analog module with up to 32 Input (3xxxxx) registers and 32 Output (4xxxxx) registers, or as a discrete module with up to 512 input bits (1xxxxx) and 512 coils (0xxxxx). The first of these Output registers (16 bits) configures the QSPXM and the others are mapped to Seriplex peripherals. The first of the Input registers (16 bits) provides a bit-map of the status of the QSPXM. The layout of the I/O registers depends on the configuration register value. The QSPXM supports lengths of the Seriplex bus up to 256 bits in multiples of 16. The QSPXM supports multiplexing of 2, 4, 8, or 16 channels deep by up to 240 bits wide in multiples of 16 bits. Multiplexed words must be positioned on 16 bit boundaries and must occupy the highest numbered bits of the configured Seriplex address space.

Specifications

Mounting Requirements

One slot of Quantum backplane.

Maximum Required Addressing

32 Words In
32 words Out

Current Draw on Quantum Rack power supply

100 mA max. (35-50mA typical)

[1] The Local and RIO racks will support the full 32 words In and 32 words Out. The DIO interface will only support a maximum of 30 words In and 32 words Out. The GCNTFCOP.SYS file for Modsoft must be modified for use with the DIO. See Appendix B on page 29 for more information.

Operating Temperature

0 to 60 degrees C operating. -40 to 80 degrees C storage.

Humidity Rating

up to 90% noncondensing

Pressure Altitude

-200 to +10,000 feet MSL

Seriplex Communication Port

9 pin male D-connector. Variable frequency (16, 32, 64, 100) Kbaud Seriplex protocol. Supports Mode 1 and Mode 2 and Multiplexed analog I/O.

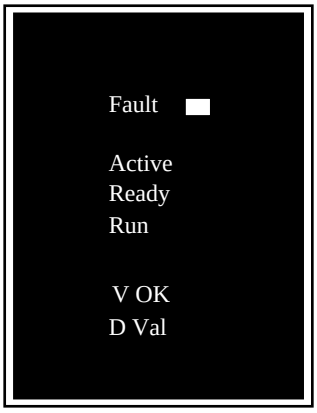
Indicator lights

6 LEDs: Green Active, Green Ready, Green Run, Green Voltage OK, Green Data Val (CDR ON) , and Red Fault

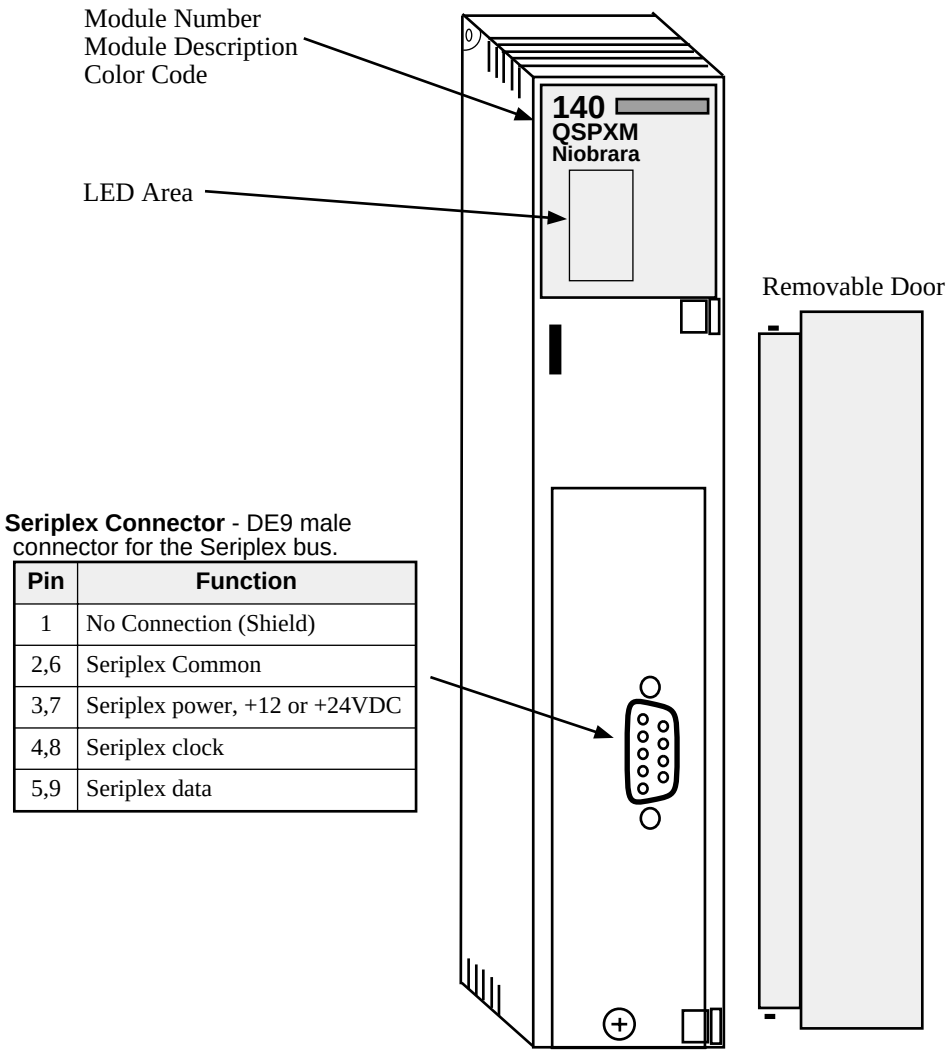
Physical Dimensions

Single width module.
Wt.:2 lb. max
W: 1.59 in.
H: 9.84 in.
D: 4.09 in.

LED Indicators and Descriptions



LED	Color	Indication when ON
Fault	Red	Seriplex Data or Clock Fault is present
Active	Green	Quantum Bus communication is present
Ready	Green	QSPXM has passed internal self checks
Run	Green	Seriplex network is active
V OK	Green	Seriplex voltage is present
D Val	Green	Seriplex CDR is active



Pin	Function
1	No Connection (Shield)
2,6	Seriplex Common
3,7	Seriplex power, +12 or +24VDC
4,8	Seriplex clock
5,9	Seriplex data

Figure 1-1 QSPXM Front Panel

2
Installation

Module Installation

Note: Like all Quantum modules, the QSPXM may be hot swapped. It is not necessary to remove power to the rack to remove or install the QSPXM.

1 Mount the QSPXM at an angle onto the two hooks near the top of the backplane slot. Rotate the module down to make electrical contact to the backplane. Secure the screw at the bottom of the module.

2 With power applied to the rack, all LEDs should strobe and when finished, the green Ready LED should illuminate and remain lit. This indicates that the QSPXM has passed its internal self checks and is ready.

3 If the Quantum CPU is in RUN, the green Active LED should illuminate. The green RUN LED will come on only when a valid configuration is loaded in the first output register and there are no Seriplex fault conditions.

4 The green V OK LED will be OFF to indicate an undervoltage on the Seriplex network. This light will come on when the Seriplex network is properly connected.

Seriplex installation

Seriplex Connector

The QSPXM connects to the Seriplex network using its 9 pin port. The pinout of this connector and the suggested wire colors for the Seriplex network cable is shown in Table 2-1.

Table 2-1 QSPXM Seriplex Connector

Pin	Function	Suggested Wire Color
1	No Connection (Shield)	Bare
2,6	Seriplex Common	Black
3,7	Seriplex power, +12 or +24VDC	Red
4,8	Seriplex clock	Green or Blue
5,9	Seriplex data	White

Seriplex Power Supply

An isolated 24VDC (or optionally 12VDC) power supply is required for the Seriplex network. The power supply requirements are listed in Table 2-2. It is recommended that the current capacity be rated at 1.2 times the total load current of the network. Also, long cable runs may result in voltage drop, so multiple power supplies may need to be included in the network.

Table 2-2 Seriplex 24V Power Supply Requirements

Characteristic	Value
Maximum Voltage	30.0 VDC (including ripple)
Minimum Voltage	19.2 VDC (including ripple)
Maximum Ripple	2.0 V peak-to-peak 47 to 378 Hz
Minimum Hold-up Time	Application-dependent
Maximum Rise/Fall Time	1 data frame period

Seriplex Clock Module

The QSPXM provides the clock signal for the Seriplex network in Mode 1 and Mode 2.

NOTE: Any external clock module is not required and should NOT be used.

Modsoft Configuration

The QSPXM requires a maximum of 32 words of Input and 32 words of Output assigned to it by the CPU. This assignment is accessed like other I/O modules through the Configure, Quantum I/O screen in Modsoft, Concept, or other programming software. The first Input register assigned to the QSPXM provides status information about the module. Table 2-3 displays the bit map for the status register. The first Holding register (output) assigned to the QSPXM is the configuration register for the module. Table 2-4 displays the bit map for the configuration register.

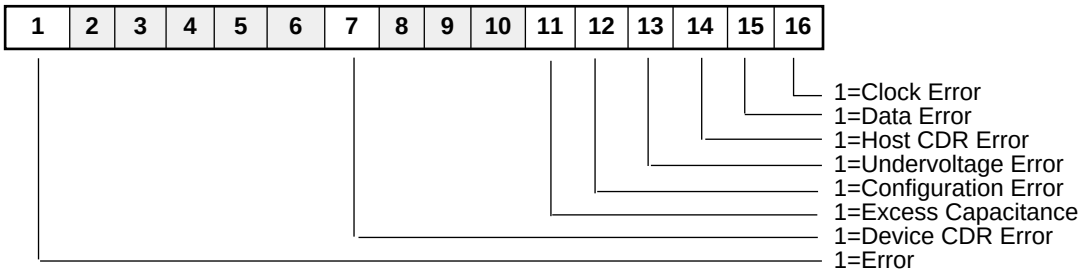
NOTE: The QSPXM uses the first 16 bits of Input assigned to its slot for status information. It does not use the 8 bit I/O Map Status Byte of the Quantum system.

NOTE: The QSPXM may be configured as a 512 contiguous discrete inputs (1x) and 512 contiguous discrete outputs (0x) or 32 contiguous input registers (3x) and 32 contiguous output registers (4x).

NOTE: In order to support analog Seriplex I/O, the Seriplex bit order will be reversed from from the Modicon bit labeling scheme but the analog values will be aligned LSB to MSB with Modicon analog registers. The inverted Seriplex bit addressing may be a source of confusion when the QSPXM is treated as a discrete module, so with the release of 04Jun98 firmware the QSPXM may be optionally configured for Modicon bit order by setting bit 3 in the configuration register.

NOTE: Modules with a revision of 08Dec98 or later have an option that, in conjunction with reversing the bit order, also shifts all of the Seriplex bits left 8 bits. To implement this, set the parameter word associated with the module to a value of 1.

Table 2-3 3x (or 1x) Input Status Word (bit 1 is msb)



The Input Status bits are set on the appropriate error condition.

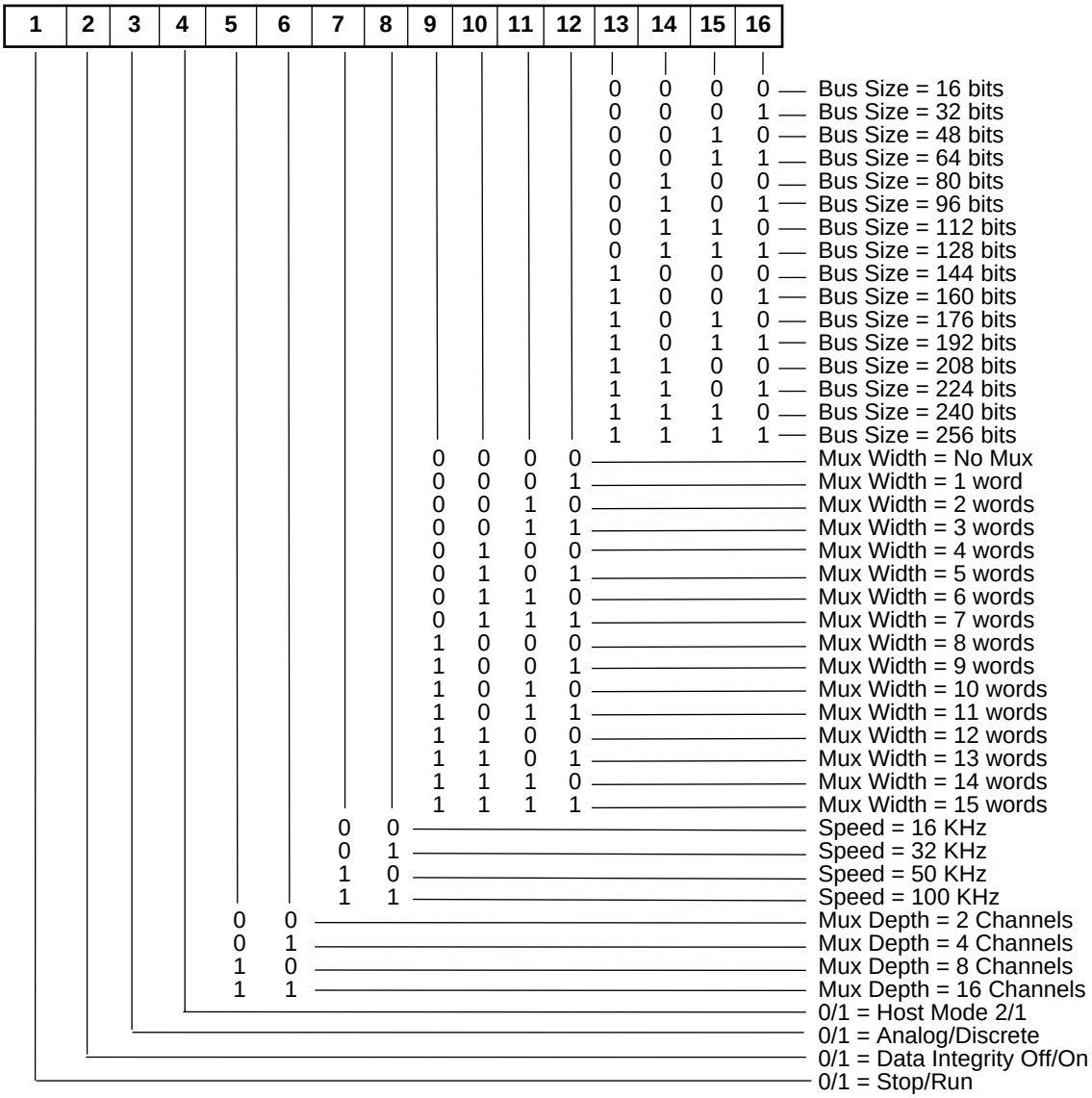
- If the QSPXM determines that the Seriplex Clock line is not responding properly (stuck high, low), then Bit 16 (lsb) will be set.
- If the data line is stuck, bit 15 will be set.
- If the Clock is shorted to Data, then both bits 16 and 15 will be set.
- If the Data Integrity (CDR) feature is enabled and a CDR error occurs at the Host, bit 14 will be set (Note: this feature is not implemented).
- If the Seriplex power voltage is below the threshold of 9 Vdc, bit 13 will be set.
- Bit 12 is set if an invalid configuration is attempted in the Configuration bits (Such as setting the MUX width wider than the network size or enabling MUX while in Discrete mode).
- If an excess capacitance is detected on the Seriplex Data Line for a give clock rate, bit 11 will be set. It will be necessary to slow down the clock rate or shorten the network cable length to fix this problem.
- If a device on the network reports a CDR error on Seriplex address 9, bit 7 of the status register will be set.
- If any of the individual errors occur, the QSPXM will halt the Seriplex bus, set the appropriate bit(s) and also set bit 1 (msb). Bit 1 may be used with a master control relay in the ladder logic. When the error condition is cleared, and bit 1 (RUN) in the configuration register is set, the Seriplex network will be restarted and the appropriate error bits cleared.

The first output word assigned to the QSPXM sets the configuration of the QSPXM.

- Bit 1 sets the RUN/STOP of the Seriplex network. Normally, bit 1 will be set ON to enable the network. The RUN light on the front of the QSPXM will be on if bit 1 is set and there are no errors. To clear an error, toggle bit 1 from ON to OFF and then back to ON.
- Bit 2 enables CDR Data Integrity. 0=Normal CDR OFF, 1=CDR ON.
- Bit 3 sets the normal Analog bit alignment or the Discrete bit alignment. When bit 3 is clear (0), then the Seriplex network bits align MSB to LSB with the Modicon bits on normal word boundaries. Seriplex address start at bit 0 while Modicon addresses start at bit 1. Also, Modicon increments its address from MSB to LSB while Seriplex increments its addresses from LSB to MSB. Therefore, Seriplex bit 16 corresponds to Modicon bit 32 and Seriplex bit 31 is the same as Modicon bit 17.

  When bit 3 is set (1), then the QSPXM changes the bit mapping to align the Seriplex address to the Modicon discrete address. This is accomplished by reversing the bit order and shifting everything by one address. Seriplex address 16 is no longer accessible by the Quantum PLC since the first PLC address is 17. Also the byte boundaries no longer match so the Multiplex modes are not allowed. This feature is intended for the simple applications of only discrete I/O. If multiplexing or analog values are needed then bit 3 must be cleared and the normal analog mapping must be used.
- Bit 4 sets the Host/Peer mode of the network. When cleared (0), the Host Controlled Mode 2 is selected. When set (1), the Peer Controlled Mode 1 is selected.
- Bits 5 and 6 set the Multiplex depth for the network.
- Bits 7 and 8 set the network clock speed.
- Bits 9, 10, 11, and 12 set the Multiplex Width.
- Bits 13, 14, 15, and 16 set the network size.

Table 2-4 4x (or 0x) Configuration Word (Bit 1 is msb)



The layout of the remaining registers of the QSPXM depends on the configuration. Following the configuration register and status register, there is one word for each non-multiplexed word (or fraction) of I/O. In mode 2, the input register indicates the state of input points on the bus (even clock cycles) and the output register determines the driven state of output modules (odd clock cycles). In mode 1, the input registers reflect the state of the Seriplex bits whether driven by modules on the bus or by the QSPXM and the output registers are wire-ored with field inputs occupying the same addresses.

NOTE: The QSPXM does not allow access to Seriplex bits 0 through 15. Registers 3x+1 and 4x+1 start with Seriplex bits 16 through 31 inclusive. The bit order is aligned LSB to MSB with the Modicon analog registers as shown in Tables 2-5 and 2-6 (Control Register bit 3 is OFF).

NOTE: If Control Register bit 3 is set ON then the register mapping is bit aligned with the Modicon bit ordering sequence starting at address 17.

Table 2-5 3x+1 Input Register

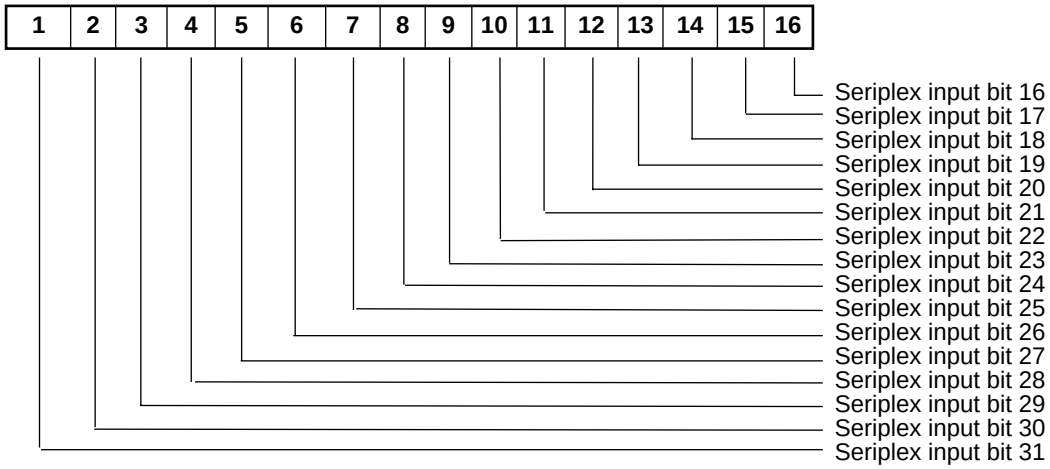
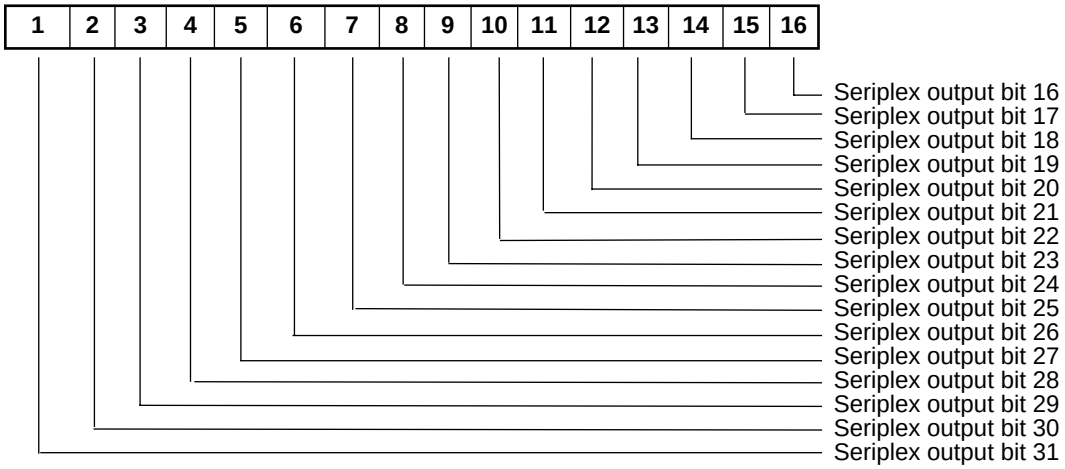


Table 2-6 4x+1 Output Register



Following the non-multiplexed registers are registers for the configured number of multiplexed words. The behavior of these bits is similar to the non-multiplexed bits described above, including mode 1 and mode 2 operations, but the scan rate is slower, being divided between the multiplexed channels. Within the banks of input and output registers, all of the channels of the first module appear followed by all of the channels of each additional module.

The QSPXM only has 31 Seriplex data registers so it is possible to configure a multiplexed network that is larger than may be mapped to the Quantum. In this case, the QSPXM truncates the data presented to the PLC, sends zero data to the multiplexed devices above the addressed area and discarding input data that may not be mapped to the Quantum.

If the PLC is halted, all Seriplex outputs will be set to zero (i.e. Seriplex data line allowed to float high). In the case of a Seriplex fault detected by the QSPXM, the red Fault LED indicator on the front of the QSPXM will light. The QSPXM can detect undervoltage, clock shorted low, clock shorted high, data shorted low, data shorted high, excess Data line capacitance, and external clock source error conditions.

Please note that, in mode 1, output disable from the PLC will not turn off any outputs driven directly by Seriplex inputs. Configuration register bit 1 can be cleared to set all outputs to their shelf state.

Configuration of the QSPXM is fully dynamic. It is not even necessary to halt the Seriplex bus before modifying bits 2 through 16 of the configuration register. Of course, if the new configuration doesn't match the hardware, you could halt the PLC with an error. For example, driving mode 1 modules with a mode 2 host can result in a bus fault.

3

Examples

Example 1, Simple Analog Configuration

This example covers a very simple Seriplex system consisting of eight Seriplex discrete I/O modules, a single 8 bit analog output module, and a Seriplex power supply. The system will be configured in mode 2 for independent inputs and outputs under host control and will be clocked at 50 KHz. The for simplicity the QSPXM has been I/O configured for Input registers 300001...300032 and Holding registers 400001...400032.

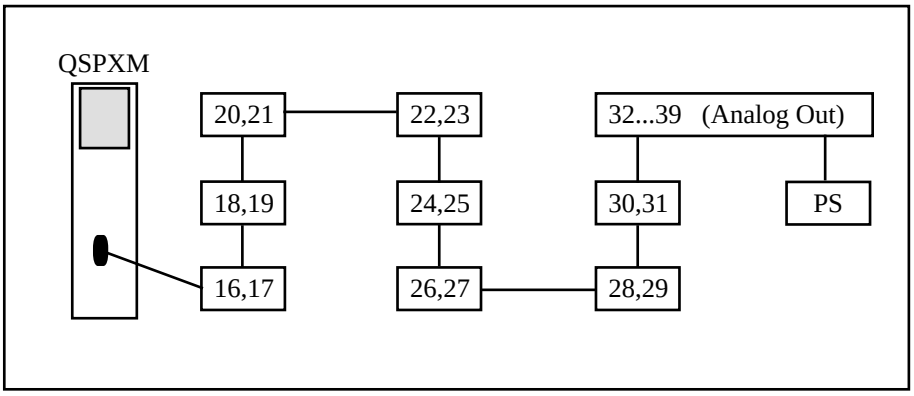


Figure 3-1 Example 1

The discrete I/O modules occupy a total of 16 bits of non-multiplexed I/O comprising two bits (A and B) for each Seriplex module. The first available Seriplex address from the QSPXM is bit 16 so the sixteen I/O points will be assigned Seriplex addresses of 16 through 31 inclusive. The 8 bit analog output module uses 8 contiguous Seriplex address and must start on an 8 bit boundary. It will occupy the Seriplex addresses 32 through 39 inclusive where bit 32 is the lsb and bit 39 is the msb. The QSPXM bus size must be programmed in multiples of 16 bits, so the QSPXM must be configured for at least 48 bits of non-multiplexed I/O. Since there are no input devices on Seriplex address 32...47, this simple configuration will only use two of the 32 input and three of the 32 output registers assigned to the module. Bits 1 though 16 of registers 300002 and 400002 will correspond to the Seriplex addresses 31 through 16. Bits 9 through 16 of register 400002 will control the analog module. The remaining bits of the 32 input and output registers will be zeroed and should be ignored by the PLC application. (See Table 3-2)

The Configuration register 400001 should be set to the value 33282 (decimal) = 8202 (hex) = 1000001000000010 (binary). This will place the network in RUN at 50KHz with a size of 48 bits. Table 3-1 displays the bit values for the Configuration register 400001.

Table 3-1 Example 1 4x Configuration Register

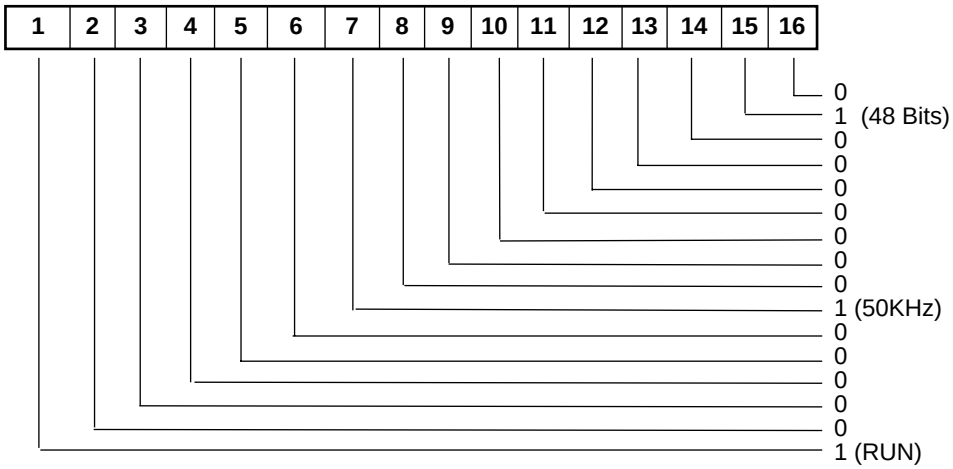


Table 3-2 Example 1 Register List

Input Register	Holding Register	1 msb	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16 lsb
300001	400001	Status register and Configuration Register															
300002	400002	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
300003	400003	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
300004..300032	400004..400032	Undefined															

The QSPXM has been assigned as an analog module so the ladder program will likely be written to use the NOBT, NCBT, NBIT, SBIT, and RBIT instructions for direct bit manipulations of the analog registers. The BLKM and other transfer blocks may also be used to move the analog values into discrete locations to simplify the ladder code. Example 2 shows this same system as a discrete configuration.

Figure 3-2 shows a simple ladder segment that uses the 16 bit ADD block to hard-code the configuration register, copies Seriplex input bit #17 to Seriplex output bit #28, and copies the analog input register 300115 to the Seriplex analog output module.

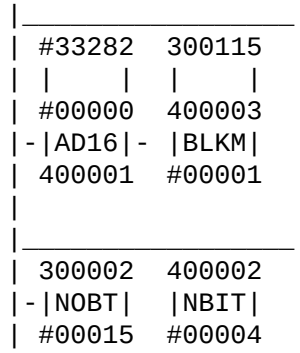


Figure 3-2 Example 1 Ladder Code

Example 2, Simple Discrete Configuration

This example covers a Seriplex system of consisting of 21 Seriplex discrete I/O modules and a Seriplex power supply. The system will be configured in mode 2 for independent inputs and outputs under host control and will be clocked at 50 KHz. The QSPXM will be configured as a discrete module with the inputs at 100001...100512 and the outputs at 000001...000512 and the Bit 3 of the Control Word will be set for discrete bit alignment.

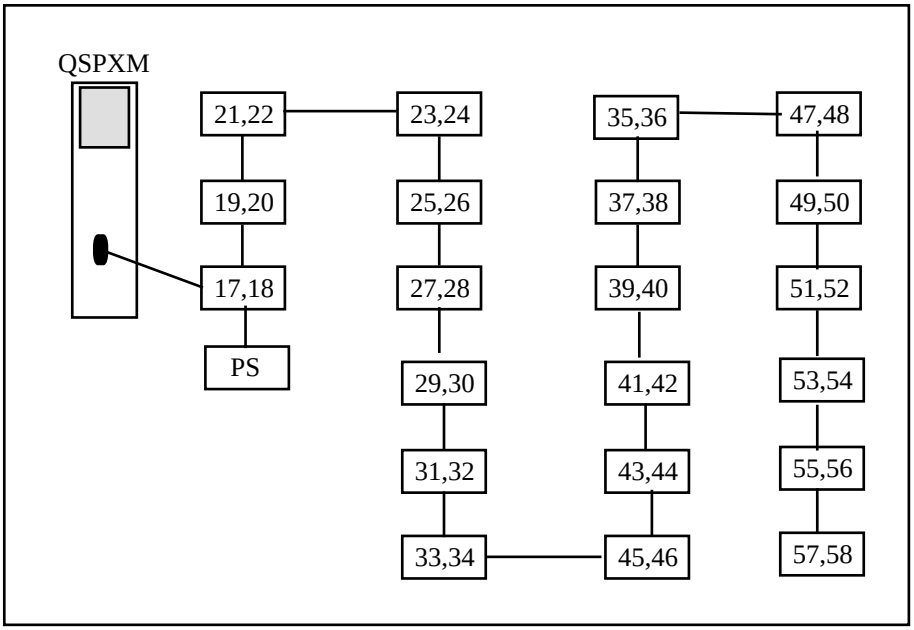


Figure 3-3 Example 2

The discrete I/O modules occupy a total of 42 bits of non-multiplexed I/O comprising two bits (A and B) for each Seriplex module. The first available Seriplex address from the QSPXM is bit 16 so the 42 I/O points will be assigned Seriplex address of 16 through 57 inclusive. The QSPXM bus size must be programmed in multiples of 16 bits, so the QSPXM must be configured for at least 64 bits of non-multiplexed I/O. The first 16 bits will be the configuration and status for the QSPXM. The next sixteen bits will be for Seriplex addresses 17..32 while the following 16 bits will be for Seriplex addresses 33...48, followed by bits 49...64. The remaining bits of the 512 inputs and outputs will be zeroed and should be ignored by the PLC application. (See Table 3-2)

Notice that Seriplex bit 16 is not available and that the Modicon byte boundaries are not aligned with the Seriplex byte boundaries because the Modicon addresses start at 1 and the Seriplex address starts at 0.

The Configuration bits 1010001000000011 (binary). This will place the network in RUN at 50KHz with a size of 64 bits. Table 3-1 displays the bit values for the Configuration.

Table 3-3 Example 2 0x Configuration Register

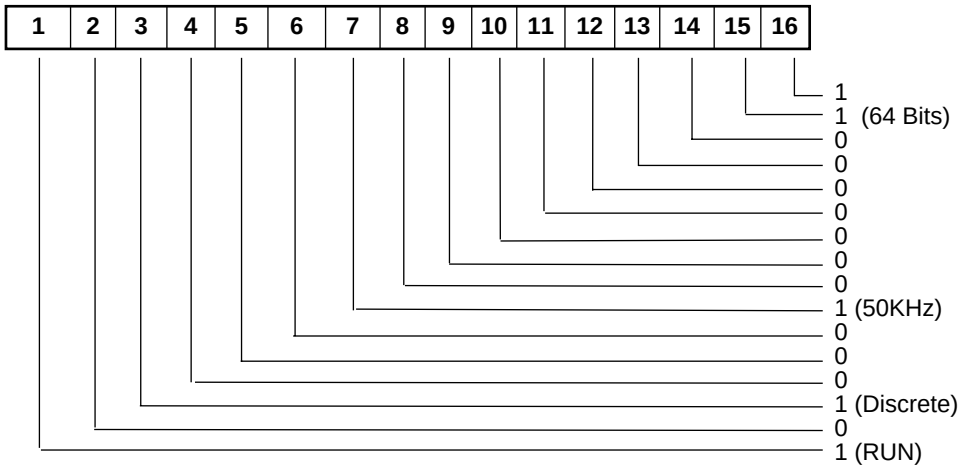


Table 3-4 Example 2 Bit List

Input Bits	Output Coils	Seriplex Addresses															
100001..100016	000001..000016	Status and Configuration															
100017..100032	000017..000032	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
100033..100048	000033..000048	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
100049..100064	000049..000064	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
100065..100512	000065..000512	Undefined															

Figure 3-4 shows a simple ladder segment that uses the 16 bit ADD block to hard-code the configuration register, copies Seriplex input bit #31 to Seriplex output bit #20.

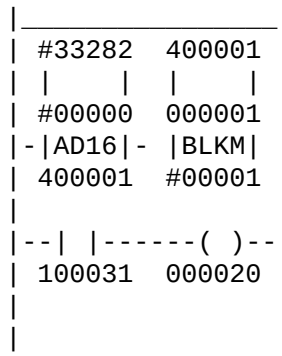


Figure 3-4 Example 2 Ladder Code

Example 3, Multiplexed System

Systems implementing Multiplexed Seriplex modules are configured much like the non-multiplexed systems. The non-multiplexed bits start at Seriplex bit 16 and go up while the multiplexed words start at the end of the network and towards the beginning

For this example there are 8 multiplexed temperature sensors with four channels per device. Since there are four analog values per device, the Mux depth should be set to 4 (bit 6 ON and bit 5 OFF in the

configuration register). The Mux Width should be set to 8 words since there are 8 devices (bit 12 OFF, bit 11 OFF, bit 10 OFF, and bit 9 ON in the configuration register). There are also 6 discrete non-multiplexed devices on the network (12 bits).

The discrete non-multiplexed devices need 12 bits and may be placed in Seriplex addresses 16 through 27 inclusive. The 8 sixteen bit words of multiplexing account for 128 bits of the Seriplex bus and must start on a 16 bit boundary. Therefore the multiplexing may start at Seriplex bit 32 and continue through bits 160. The bus length will be set for 160 bits (bit 16 ON, bit 15 OFF, bit 14 OFF, and bit 13 ON).

This system will be configured for Mode 2 (bit 4 OFF) and for RUN (bit 1 ON). The network speed only needs to be 16kHz (bit 8 OFF, bit 7 OFF).

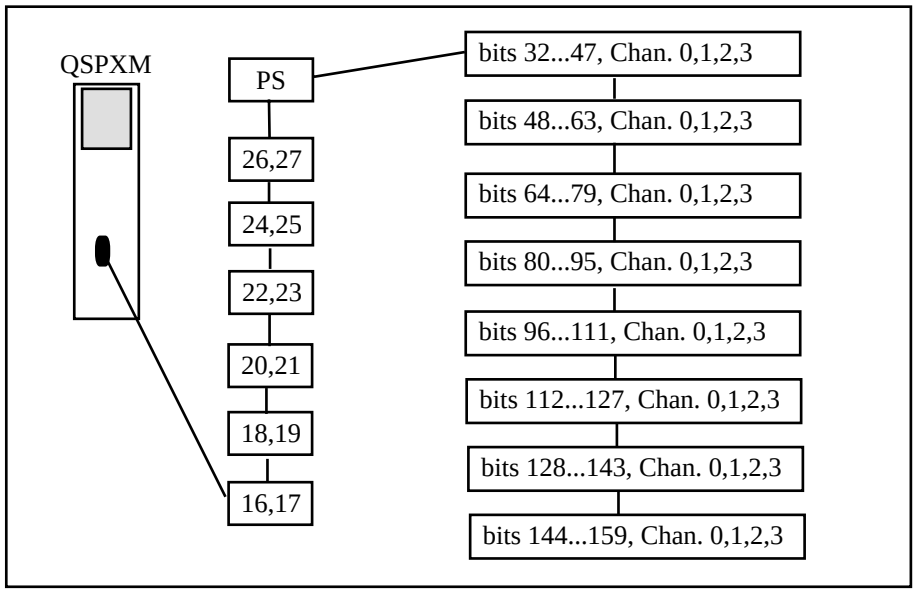


Figure 3-5 Example 3

The resulting value for the Configuration register is 33929 (decimal) = 8489 (hex) = 1000010010001001 (binary). The QSPXM is assigned as analog registers by the PLC. The tables below describe the register format for the inputs and outputs at the PLC where QSPXM has been assigned addresses 300001...300032 and 400001...400032.

Notice that the Seriplex setup is larger than the 32 registers available to the PLC. This means that Channels 2 and 3 of the module with Seriplex addresses 144...159 will not be accessed by the PLC. Their inputs will be ignored by the QSPXM and their outputs will be set to zero.

Table 3-5 Example 3 Input Registers

PLC Register	Seriplex Description
300001	Seriplex Status Word
300002	Non-multiplexed Seriplex Inputs 31...16
300003	Multiplexed Seriplex Inputs 47...32 Channel 0
300004	Multiplexed Seriplex Inputs 47...32 Channel 1
300005	Multiplexed Seriplex Inputs 47...32 Channel 2
300006	Multiplexed Seriplex Inputs 47...32 Channel 3
300007	Multiplexed Seriplex Inputs 63...48 Channel 0
300008	Multiplexed Seriplex Inputs 63...48 Channel 1
300009	Multiplexed Seriplex Inputs 63...48 Channel 2
300010	Multiplexed Seriplex Inputs 63...48 Channel 3
300011	Multiplexed Seriplex Inputs 79...64 Channel 0
300012	Multiplexed Seriplex Inputs 79...64 Channel 1
300013	Multiplexed Seriplex Inputs 79...64 Channel 2
300014	Multiplexed Seriplex Inputs 79...64 Channel 3
300015	Multiplexed Seriplex Inputs 95...80 Channel 0
300016	Multiplexed Seriplex Inputs 95...80 Channel 1
300017	Multiplexed Seriplex Inputs 95...80 Channel 2
300018	Multiplexed Seriplex Inputs 95...80 Channel 3
300019	Multiplexed Seriplex Inputs 111...96 Channel 0
300020	Multiplexed Seriplex Inputs 111...96 Channel 1
300021	Multiplexed Seriplex Inputs 111...96 Channel 2
300022	Multiplexed Seriplex Inputs 111...96 Channel 3
300023	Multiplexed Seriplex Inputs 127...112 Channel 0
300024	Multiplexed Seriplex Inputs 127...112 Channel 1
300025	Multiplexed Seriplex Inputs 127...112 Channel 2
300026	Multiplexed Seriplex Inputs 127...112 Channel 3
300027	Multiplexed Seriplex Inputs 143...128 Channel 0
300028	Multiplexed Seriplex Inputs 143...128 Channel 1
300029	Multiplexed Seriplex Inputs 143...128 Channel 2
300030	Multiplexed Seriplex Inputs 143...128 Channel 3
300031	Multiplexed Seriplex Inputs 159...144 Channel 0
300032	Multiplexed Seriplex Inputs 159...144 Channel 1

Table 3-6 Example 3 Output Registers

PLC Register	Seriplex Description
400001	Seriplex Configuration Word = 33929 decimal
400002	Non-multiplexed Seriplex Outputs 31...16
400003	Multiplexed Seriplex Outputs 47...32 Channel 0
400004	Multiplexed Seriplex Outputs 47...32 Channel 1
400005	Multiplexed Seriplex Outputs 47...32 Channel 2
400006	Multiplexed Seriplex Outputs 47...32 Channel 3
400007	Multiplexed Seriplex Outputs 63...48 Channel 0
400008	Multiplexed Seriplex Outputs 63...48 Channel 1
400009	Multiplexed Seriplex Outputs 63...48 Channel 2
400010	Multiplexed Seriplex Outputs 63...48 Channel 3
400011	Multiplexed Seriplex Outputs 79...64 Channel 0
400012	Multiplexed Seriplex Outputs 79...64 Channel 1
400013	Multiplexed Seriplex Outputs 79...64 Channel 2
400014	Multiplexed Seriplex Outputs 79...64 Channel 3
400015	Multiplexed Seriplex Outputs 95...80 Channel 0
400016	Multiplexed Seriplex Outputs 95...80 Channel 1
400017	Multiplexed Seriplex Outputs 95...80 Channel 2
400018	Multiplexed Seriplex Outputs 95...80 Channel 3
400019	Multiplexed Seriplex Outputs 111...96 Channel 0
400020	Multiplexed Seriplex Outputs 111...96 Channel 1
400021	Multiplexed Seriplex Outputs 111...96 Channel 2
400022	Multiplexed Seriplex Outputs 111...96 Channel 3
400023	Multiplexed Seriplex Outputs 127...112 Channel 0
400024	Multiplexed Seriplex Outputs 127...112 Channel 1
400025	Multiplexed Seriplex Outputs 127...112 Channel 2
400026	Multiplexed Seriplex Outputs 127...112 Channel 3
400027	Multiplexed Seriplex Outputs 143...128 Channel 0
400028	Multiplexed Seriplex Outputs 143...128 Channel 1
400029	Multiplexed Seriplex Outputs 143...128 Channel 2
400030	Multiplexed Seriplex Outputs 143...128 Channel 3
400031	Multiplexed Seriplex Outputs 159...144 Channel 0
400032	Multiplexed Seriplex Outputs 159...144 Channel 1

4

Connector Pinouts

Seriplex Port (DE9P with jack screw posts)

Pin	Function	Color
1	No Internal Connection. May be used for Seriplex Shield	Bare
2,6	Seriplex Common	Black
3,7	Seriplex power, +12 or +24VDC	Red
4,8	Seriplex clock	Green or Blue
5,9	Seriplex data	White

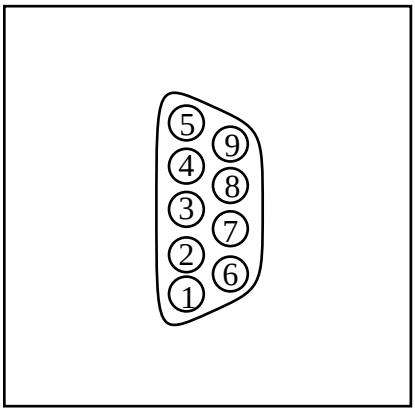


Figure 4-1 Seriplex Connector Pinout

5
Trouble Shooting

V OK off

When the voltage on the Seriplex network falls below the minimum working range, the green V OK light goes off. Undervoltages may occur due to a cable break between the QSPXM and the Seriplex power module, a loss of power to the power module, a cable short somewhere on the network, or a faulty power module. A DC voltage meter is a handy tool for tracing power problems.

After the undervoltage problem is solved, the QSPXM will automatically restart the Seriplex bus as long as a good configuration is in Holding register 1 and the PLC is in RUN.

When the V OK light is off, the RUN light on the QSPXM will be off. The Seriplex network will not run while a fault condition exists within the QSPXM. All Seriplex devices will revert to their programmed default state.

Fault

In addition to the Undervoltage condition, the QSPXM can detect the following:

- Clock shorted low
- Clock shorted high
- Data shorted low
- Data shorted high
- Clock shorted to Data
- External clock active on the network
- Excess Data Line Capacitance for a given clock rate
- Running Mode 1 devices with a Mode 2 Host may sometimes generate a Fault. Especially at a high clock rate (100kHz).

If any of these situations occur, the red Fault light will be lit, the appropriate error bit will be set in the first input register assigned to the QSPXM, and the Seriplex network will stop. When the Fault light is on, the RUN light on the QSPXM will be off. The Seriplex network will not run while a fault condition exists within the QSPXM. All Seriplex devices will revert to their programmed default state.

Appendix A
NR&D Internet

Niobrara is on the World Wide Web! Visit our home page at **http://www.niobrara.com** to see product information, cutsheets, application notes, and ftp current software releases.

Technical support questions may be E-mailed to

techsupport@niobrara.com

Marketing questions may be E-mailed to:

marketing@niobrara.com

Additional information about Seriplex may be found at **www.seriplex.org**.

Additional information about the Quantum may be found at **www.modicon.com**.

Appendix B
Modsoft Traffic Cop Configuration

The register configuration of the QSPXM is governed by its entry in the Traffic Cop description and characteristic file: GCNFTCOP.SYS. This file is typically located in the \MODSOFT\RUNTIME directory.

NOTE: Pay special notice to the warning about editing this file with editors that do not support line width greater than 255 characters.
DO NOT use MS-DOS EDIT on this file!

The entry for the QSPXM follows the form of a Quantum Dual Port Memory I/O module with 64 bytes of input and 64 bytes of output. The standard entry used in Modsoft V2.4 is shown below:

```
QSPXM     ,214,0,64,64,NR&D Q Seriplex,0,L012F,2,0000
12345678901234567890123456789012345678901234567890123
```

The fields are comma separated.

The first 10 characters are the Name of the module.

The 214 is the next entry in the list of available devices. If you are adding this line, choose the next free number in the list.

The 0 in character position 16 indicates that other modules may be inserted in this drop.

The 64 in character positions 18 and 19 set the number of INPUT bytes.

The 64 in character positions 21 and 22 set the number of OUTPUT bytes.

The next field is the text description (19 characters max.).

The 0 in position 40 determines that the module is a discrete module and may take 0x, 1x, 3x, 4x references.

The module ID is L012F.

The 2 that follows signifies that the QSPXM is a QUANTUM DPM module.

The last 0000 tells the T_MODULE.LmsSlotData.a to use the default module bits.

It is possible to modify the width of the INPUT bytes and OUTPUT bytes to adjust the QSPXM for a unique application. For instance, in Examples 1 and 2, the Seriplex network is small and only 3 words (6 bytes) of I/O was actually used of the 32 words (64 bytes) assigned. The Quantum rack only allows 64 words total for the rack so it may be desirable to reduce the number used by the QSPXM to allow for

other I/O. In Examples 1 and 2, the Input and Output bytes might be set down to 10 bytes each to allow for some future expansion of the Seriplex network and still free some I/O for other devices.

NOTE: If the entry in the Traffic Cop configuration file is altered, all QSPXMs in the PLC system will use this entry. Also, special care will be needed during future updates of Modsoft to carry the altered setting to the new revision.

Appendix C
Concept 2.1 Configuration

The register configuration of the QSPXM is governed by its entry in the Traffic Cop description and characteristic file: GCNFTCOP.SYS. This file is typically located in the \MODSOFT\RUNTIME directory.