CERI

Installation and Programming Manual

This manual covers the CERI Compact Ethernet Remote Interface.

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1 Introduction

The Niobrara CERI is a Modicon Compact 984 compatible module that replaces the Compact PLC CPU to convert the A120 Series I/O into distributed Ethernet I/O capable of remote control using Modbus/TCP. The The CERI is a standard double-width module that resides in slots 1 and 2 of the processor rack (DTA 200). The full compliment of main rack and up to three expansion racks (DTA 201 and DTA 202) are supported by the CERI. The CERI includes a 2.5A power supply powered by 24VDC.

Figure 1.1: Typical Configuration

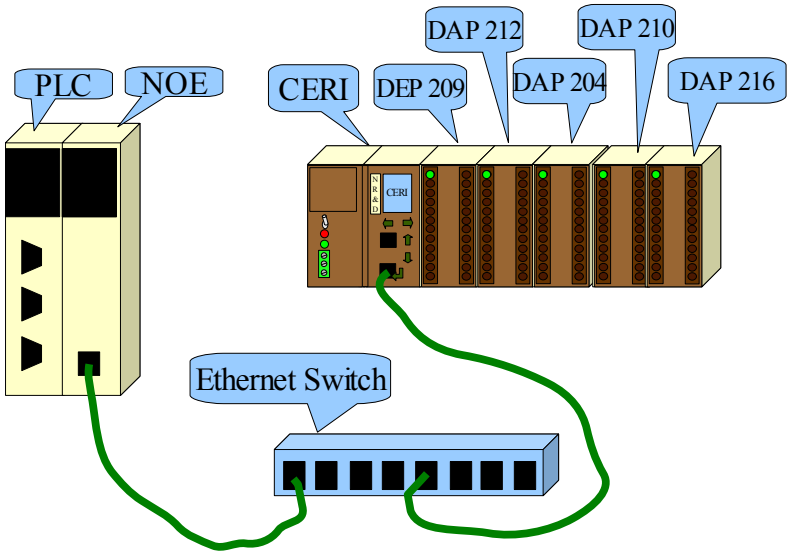


Figure 1.1 shows a typical configuration where a CERI is installed in a Compact PLC rack with A120 I/O. The primary rack contains the CERI, DEP 209, DAP 212, DAP 204 while the two-slot secondary rack contains a DAP 210 and DAP 216. The CERI is connected to a standard Ethernet switch using a normal CAT5 cable. A Quantum PLC with its own NOE Ethernet card is also connected to the Ethernet switch. The CERI is configured to map its A120 I/O into a block of 4x Holding Registers. The Quantum PLC uses the I/O Scanner feature of its NOE to communicate with the CERI to read and write the 4x registers and thus control the remote I/O. The CERI's Web page is shown in Figure 1.2.

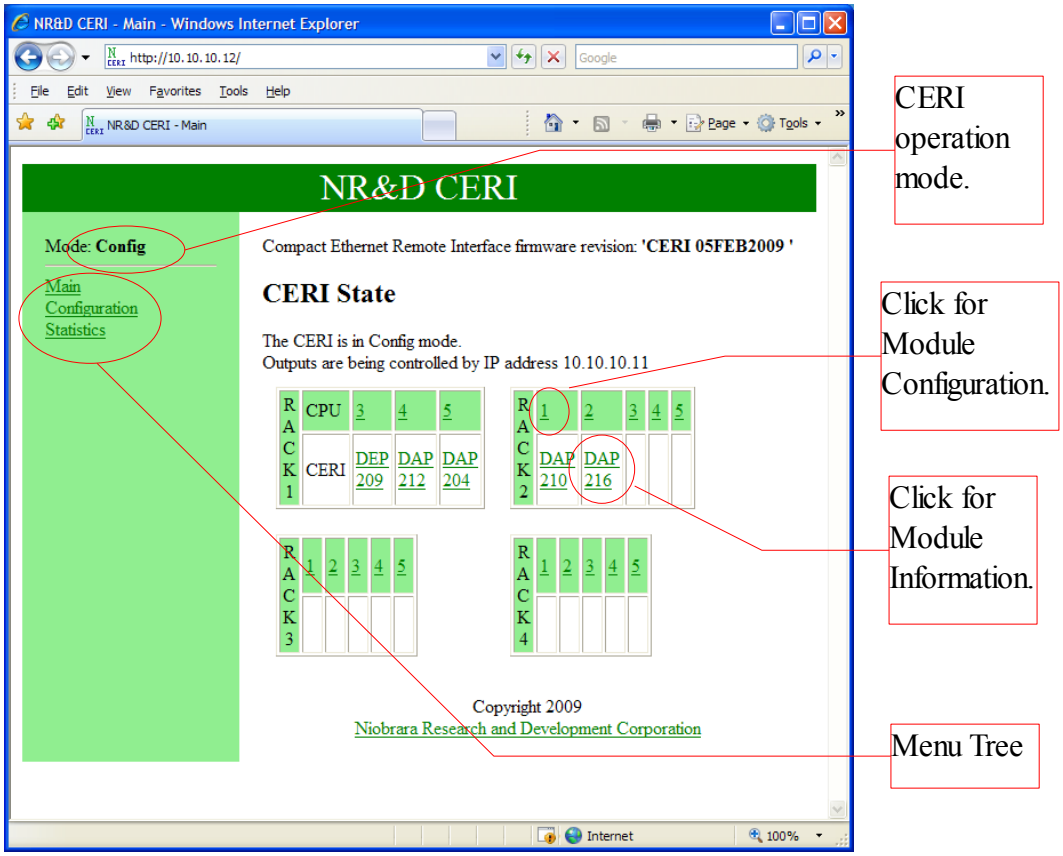


Figure 1.2: CERI Main Web Page

The Main Web page of the CERI shows each of the four possible A120 racks. The CERI is installed in the CPU slots of Rack 1. Racks 2, 3, and 4 are always displayed on the CERI's Web pages, even if they are not physically present. The CERI Web page always displays the racks in the over/under 1-2/3-4 layout regardless of the actual physical rack layout.

NOTE: Consult the Modicon 984-A120 Compact PLC User Guide (890 USE 108 00) for a complete listing of legal rack arrangements.

Figure 1.3 shows the configuration page for the DAP 212. This module includes 8 discrete inputs that are mapped to 4x register 3102 and four discrete outputs mapped to 4x register 4101. The I/O Scanner in the Quantum would simply read register 3102 from the CERI (Modbus/TCP Index 0) to gather the input values and write register 4101 to set the outputs for this car

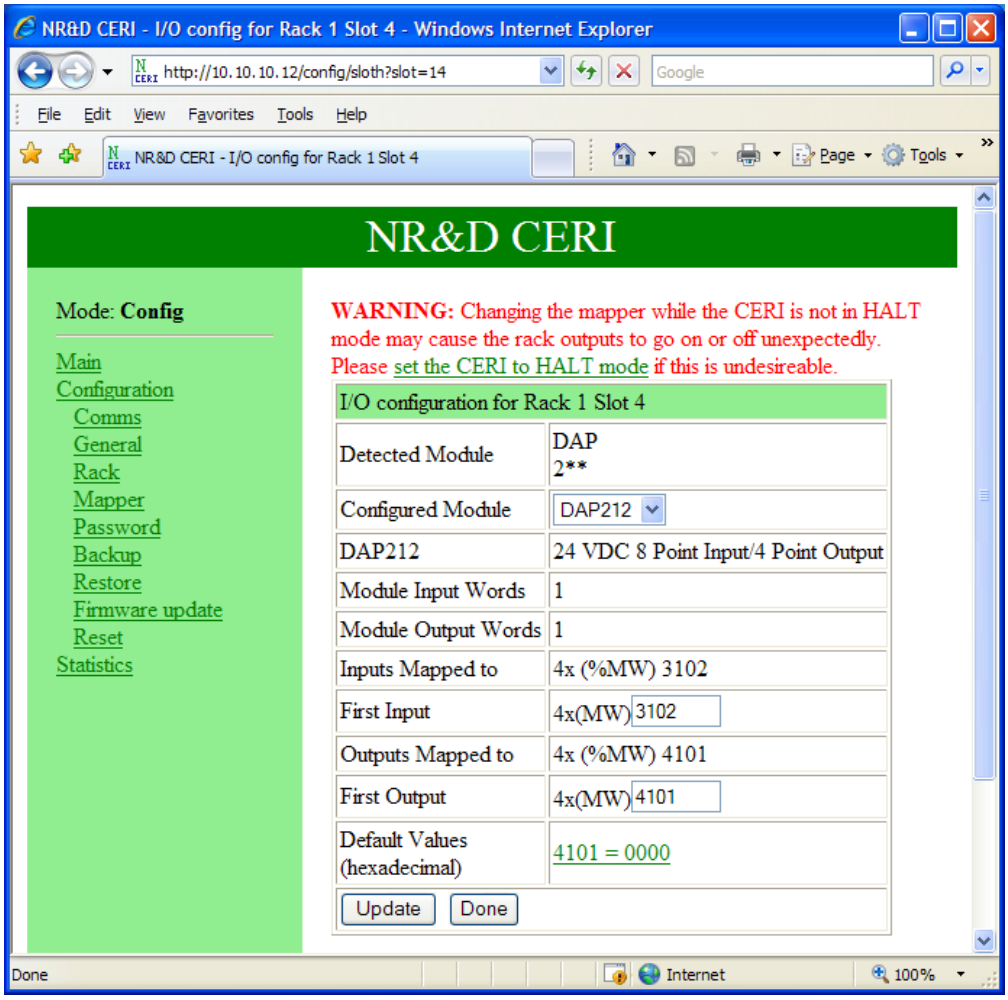


Figure 1.3: DAP212 Config Web Page

NOTE: Many A120 cards share the same Module ID so the CERI is unable to uniquely identify certain modules.

2 Installation

Module Installation

- Mount the CERI in slots 1 and 2 of a Compact processor rack (DTA 200). The Compact PLC must be removed from this slot before the CERI is installed.
- Tighten the mounting screw to ensure that the card will not accidentally be removed.
- Move the power switch on the CERI to OFF.
- Connect the 24Vdc power to the CERI removable green connector.

NOTE: It is advisable to configure the IP Address of the CERI before connecting the unit to the Ethernet network to avoid the possibility of a duplicate address with an existing Ethernet device.

- Move the CERI's power switch to ON. The LCD screen should light up and show the booting sequence. The IP Address will be displayed on the screen when the booting sequence is finished. If the IP Address does not conflict with any devices on the network then proceed to the next step, otherwise modify the address using the keys on the CERI front panel.
    - Press the ➡ key to select Setup.
    - Press the ➡ key to select Communications.
    - Press the ➡ key to select Ethernet.
    - Press the ➡ key to select the IP Address.
    - Use the arrow keys to modify the IP Address. Press the ↵ key to accept the chosen address.
    - Use the same procedure to modify the Default Gate and Subnet Mask if needed.
    - Press the ⬅ arrow to exit to the main screen.
- Connect the Ethernet port of the CERI to a switch or hub with a standard CAT5 Ethernet cable. The LINK light should illuminate on the CERI and begin flashing as Ethernet data is received by the CERI. The 100MB light will illuminate if a

100MB connection is established with the switch. The CERI may be configured to operate at 10/100MB FD/HD.

- Configure the IP Address of a PC to match the same subnet of the CERI. Be careful to set the PC to an unused IP Address to avoid a conflict. For example, if the CERI is configured for 10.10.10.10 then set the PC to 10.10.10.11.
- Ping the CERI to verify a good IP connection to the PC. Figure 2.1 shows a Command Prompt window in XP. Simply type ping followed by the target IP Address. If the target device replies then move to the next step.

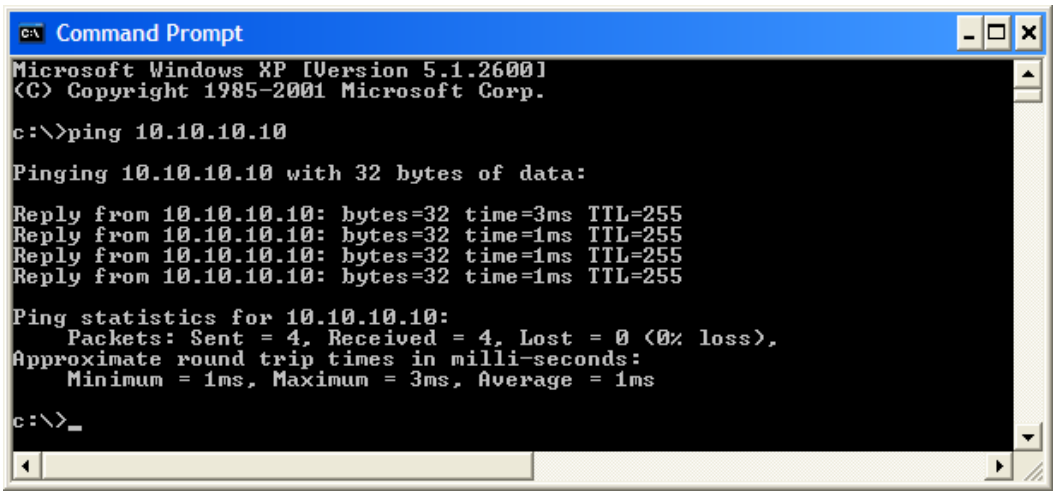


Figure 2.1: Ping 10.10.10.10

- Point a Web Browser (IE, Firefox, Opera) at the IP Address of the CERI. The page will look something like Figure 2.2 although the exact layout of detected A120 modules (in gray) will depend on the installation.
- Proceed to Chapter 3 for more information about configuration.

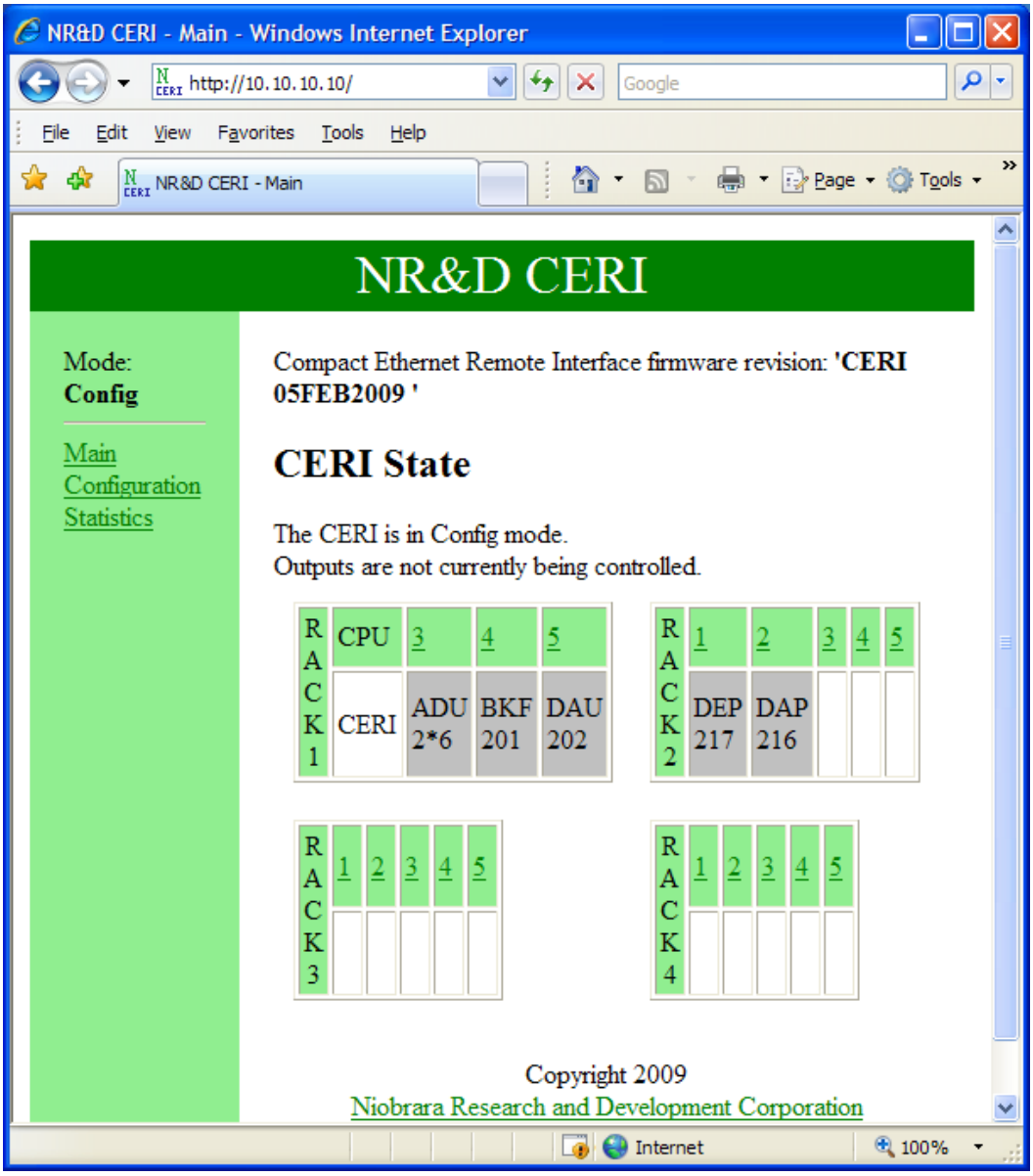


Figure 2.2: Example Default Web Page

Software Installation

The CERI_SETUP.EXE file includes this user manual, the ceri.fwl firmware file, the FWLOAD.EXE firmware loader utility, and the NRDTOOL.EXE register viewer utility. The latest version of this file is located at www.niobrara.com. Follow the link for "Download Area", select "CERI".

Power Supply

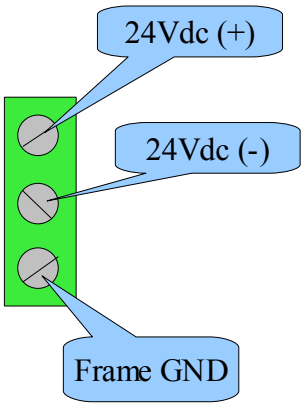
The CERI operates on 24Vdc just like the Compact PLC. The removable power supply connector pinout is shown in Figure 2.3.

The CERI includes an ON/OFF switch. This switch should be set to OFF when adding/removing A120 I/O cards to/from the rack(s).

A green “Power” LED is on when the CERI is providing 5Vdc power to the A120 rack(s).

A red “Overload” LED is on when the power load of the A120 rack(s) exceeds the rating of the CERI's power supply.

Figure 2.3 Power Connector Diagram



RS-232 Serial Port

Port 1 of the CERI is a standard Compact CPU pinout RJ45 RS-232 port. The pinout is shown in Table 2.1: RJ45 RS-232 Pinout. The Niobrara MM1 cable is used to connect Port 1 of the CERI is to the a standard 9-pin serial port on a PC. This connection would rarely be used since all features of the CERI may be accessed through the Ethernet port. This port may be used to load firmware into the CERI if an Ethernet connection is unavailable. It also supports Modbus RTU communications at a default value of 9600,E,8,1.

CERI firmware revisions 16Nov2010 or later support a unique data mailbox scheme to allow a serial Modbus master to interchange data with the new controlling CPU. This feature is extremely useful for applications with an existing Human Machine Interface (HMI) was serially connected to the old Compact CPU and now may be directly connected to the CERI. See Chapter 9 for more information.

Table 2.1: RJ45 RS-232 Pinout

Pin	Function
1	+5Vdc
2	DSR (pulled high)
3	Data TX
4	Data RX
5	Signal GND
6	RTS
7	CTS
8	Chassis GND

Figure 2.4 Serial Port Diagram

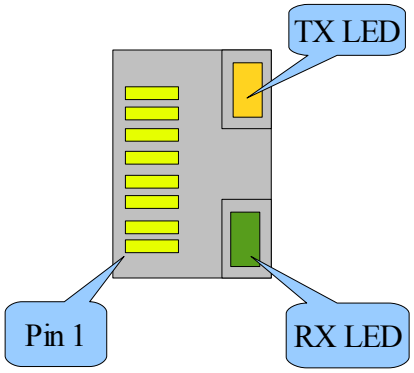
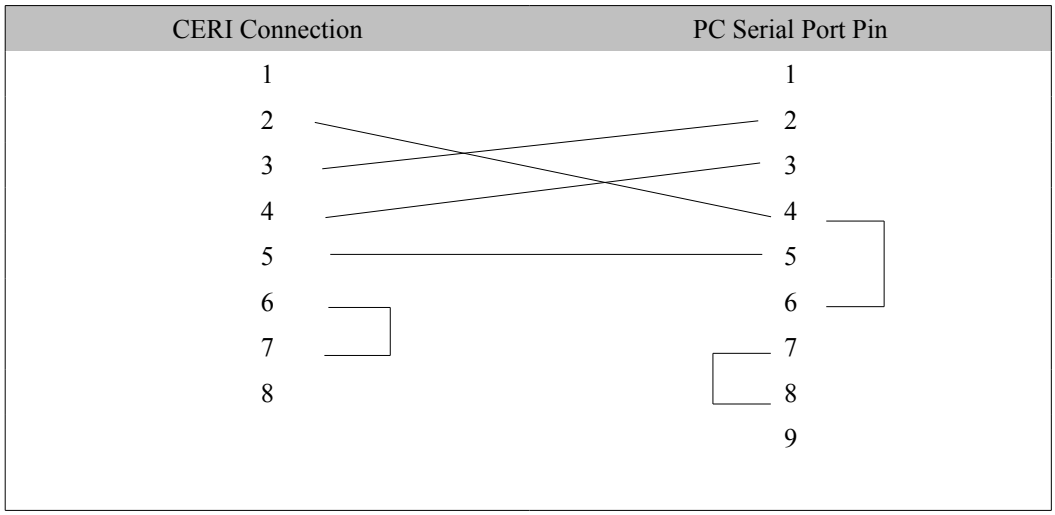


Figure 2.5.: MM1 Serial Cable



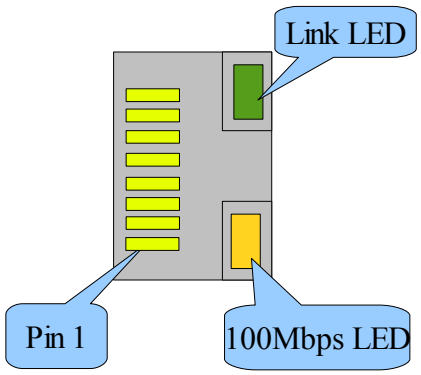
Ethernet Port

The CERI includes a standard RJ45 Ethernet port. The pinout is shown in Table 2.2: RJ45 Ethernet Pinout. Standard CAT5 cabling is used between the CERI and other Ethernet devices like a switch or hub. The green LINK LED will be on when a link is established and blinks off when data is arriving at the CERI. The CERI will automatically cross-over if needed. The amber 10/100 LED is on when the CERI is operating at 100Mbps.

Table 2.2: RJ45 Ethernet Pinout

Pin	Function
1	Transmit (+)
2	Transmit (-)
3	Receive (+)
4	Unused
5	Unused
6	Receive (-)
7	Unused
8	Unused

Figure 2.6 Ethernet Port Diagram



Updating the CERI Firmware

NOTE: Loading the CERI firmware through the serial port is not recommended. Loading firmware through the CERI's Web server is many times faster and may be done remotely. (See page 31)

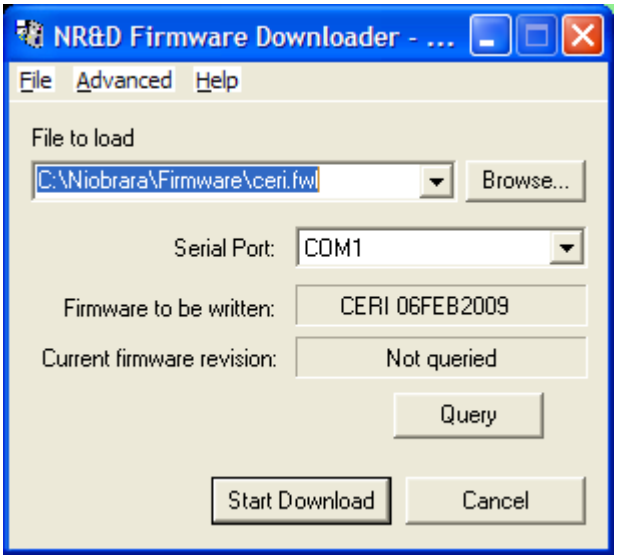
NOTE: Loading new firmware into the CERI may cause the unit to revert to factory defaults. Always perform a backup of the CERI's configuration through the Web server before preforming a firmware download.

On occasion it may be necessary to update the operating system of the CERI. The FWLOAD program is used to install the CERI firmware through the RS-232 serial port.

1. Move the power switch on the CERI to OFF.
2. Hold down the ↵ key and then move the power switch to ON. The screen on the CERI will power up and eventually show "FIRMWARE LOADER".

3. Start FWLOAD.EXE. The Windows Start Menu link is “Start, Programs, Niobrara, CERI, FWLOAD CERI Firmware”.
4. Click on the Browse button and select CERI.FWL.
5. Ensure that the proper PC serial port is selected (COM1).
6. Connect the MM1 cable from the CERI port 1 to the selected PC serial port.
7. Press the “Start Download” button. FWLOAD will open a progress bar to show the status of the download.
8. Cycle power on the CERI to return the unit to normal operation. The module is ready for use.

Figure 2.7: FWLOAD Screen



3 Web Server

Main Page

The CERI is configured using its built-in Web server. Simply enter the CERI's IP Address in a browser's URL and a page similar to Figure 3.1 should be displayed.

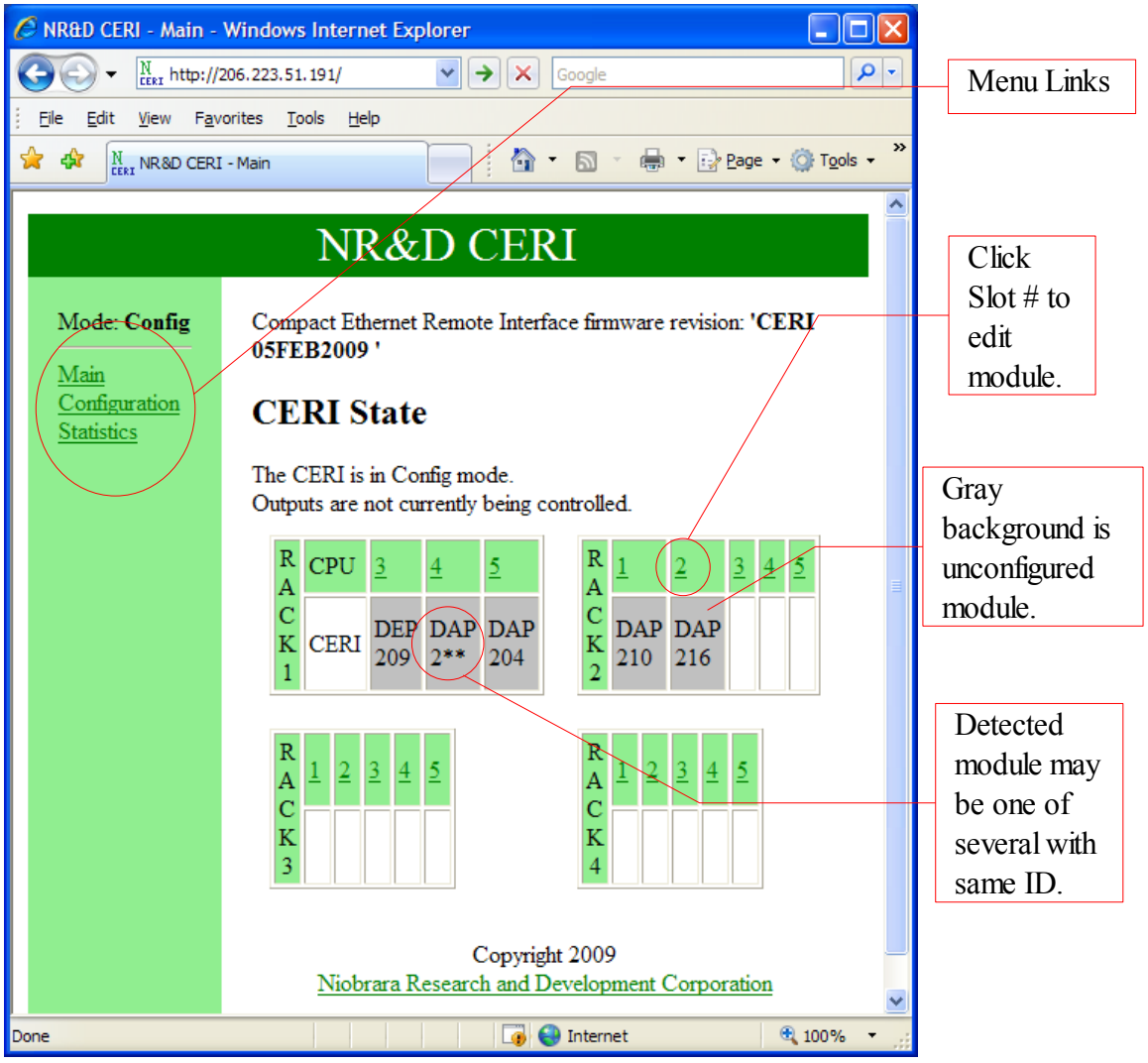


Figure 3.1: Example Main Web Page

Login

Selecting the “Configuration” link will lead to the “Configuration” page. When the “Configuration” page is first accessed on a new Web connection the user will be prompted for a user name and password as shown in Figure 3.2.

The “User name” is ignored by the CERI. The word “master” is commonly used.

The “Password” defaults to “master” and is case sensitive. This password may be changed through the Web interface.

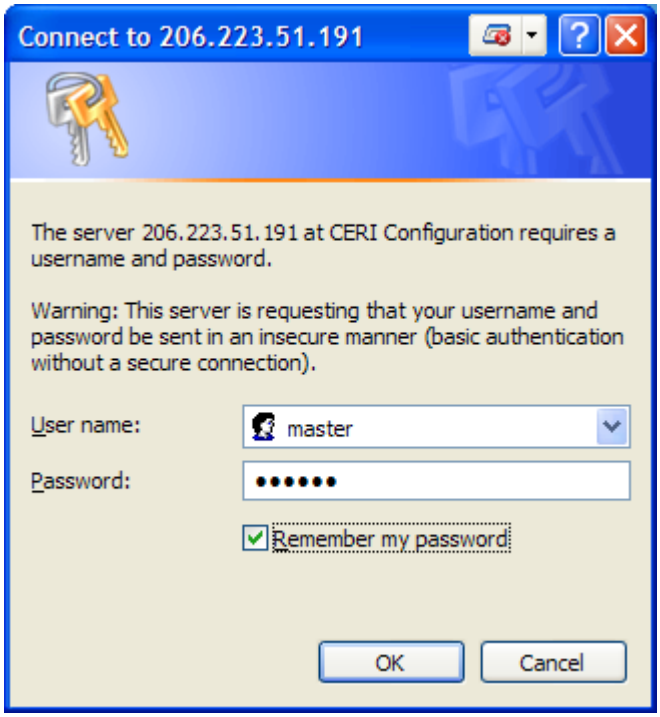


Figure 3.2: Login

The “Configuration” link should show a page similar to Figure 3.3. This page gives an overview of the CERI.

The “Communications” settings including the IP Address, Subnet Mask, Default Gateway, and Serial Port settings are shown.

The “Control” Settings gives the list of Allowed Masters and the Communications Timeout.

The “General” settings show the mode of operations and the target action on a mismatch of configuration.

The “Rack Mapping” gives an overview of the A120 I/O layout. See Chapter 4 on page 37 for more information on the Rack Mapper.

The “Internal Mapping” gives a listing of the internal map entries. See Chapter 5 on page 43 for more information on the Internal Mapper.

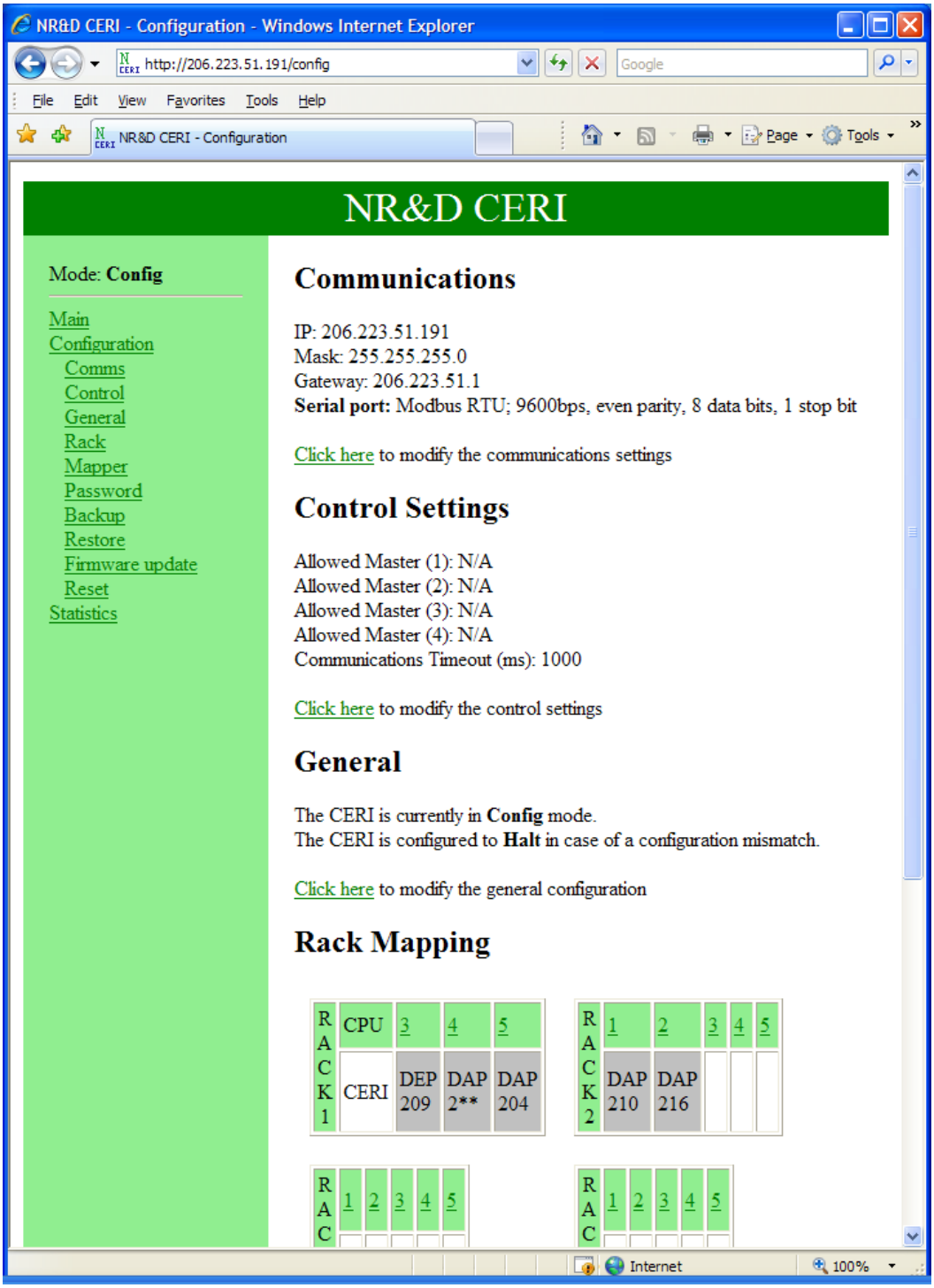


Figure 3.3: Configuration Web Page

Comms Page

A fixed IP Address may be entered through the “Comms” link. BOOTP and/or DHCP operation may also be enabled on this page. If either BOOTP or DHCP are enabled then the CERI will attempt to connect to a BOOTP or DHCP server on power-up and retrieve new IP settings. These new settings will override any fixed values until the next power cycle.

Figure 3.4: Comms Page

These settings may also be edited through the front panel of the CERI. See Chapter 7 for more information.

Control Page

The “Control” page allows the editing of the IP Addresses of the four potential controlling masters of the CERI I/O. Any client may connect to the CERI via Modbus/TCP and read the state of the I/O but only clients listed in this table will be allowed the ability to write the outputs.

The first client included in this table that sends a Modbus/TCP write to the CERI will be declared the “Controlling Master” and will have sole control of the outputs. This sole control is maintained until this master allows the “Timeout” to elapse without sending a write to the CERI. After the timeout expires, the CERI will allow any of the masters in the table to gain control.

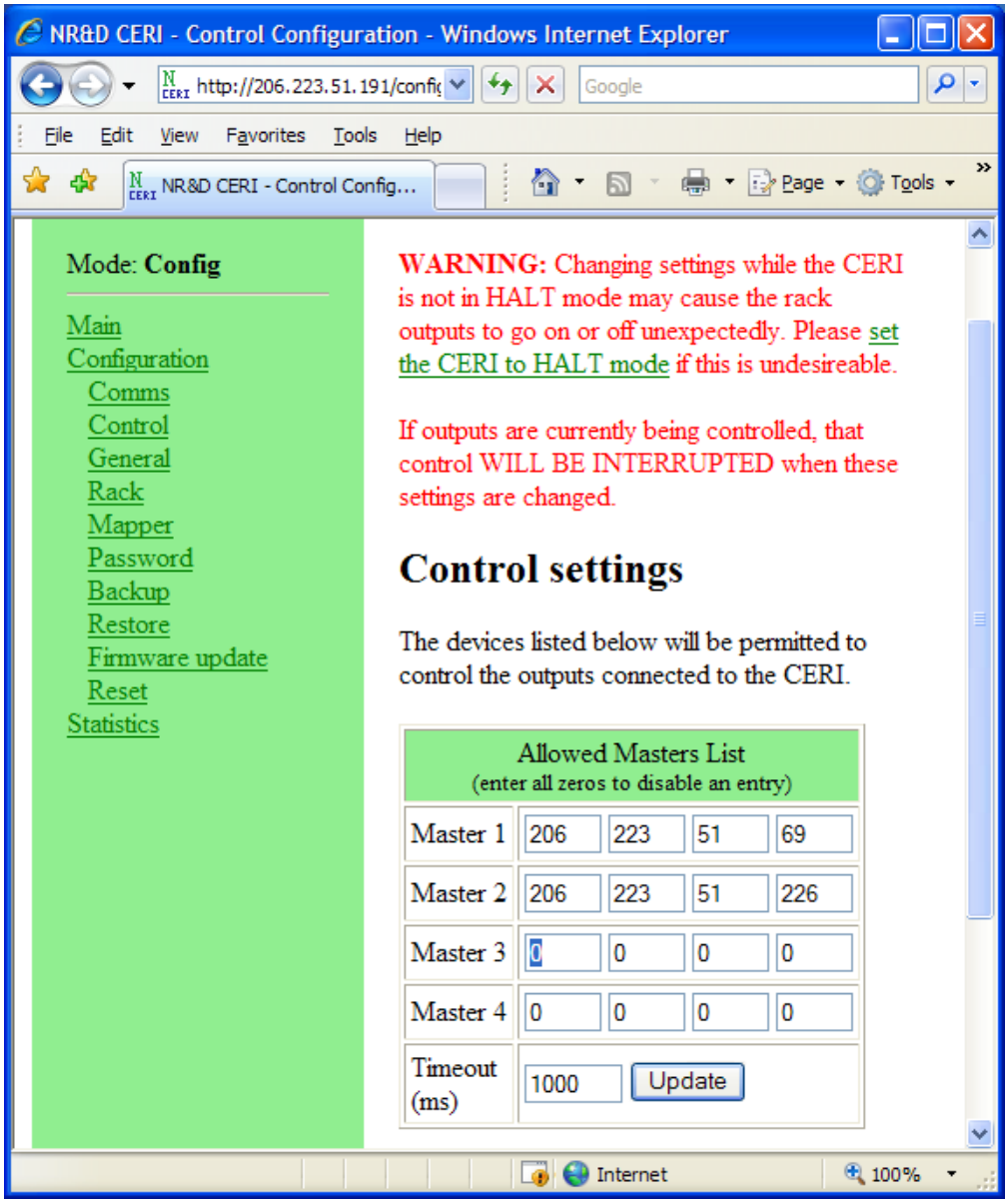


Figure 3.5: Control Page

General Configuration Page

The “General” page controls the operating mode of the CERI.

The Run Mode has options of “Config”, “Run”, and “Halt”.

- Config – This mode allows the editing of the CERI's configuration while possibly having the I/O controlled by one of the Masters.

NOTE: Changing the configuration while the outputs are being controlled may result in a temporary loss of control of the outputs resulting in equipment damage, injury or death.

- Run – This mode does not allow changes to the CERI configuration. This is effectively a 'memory protect' setting for the CERI.
- Halt – This mode forces all outputs to their default state. The CERI must be in Halt mode for a firmware upgrade.

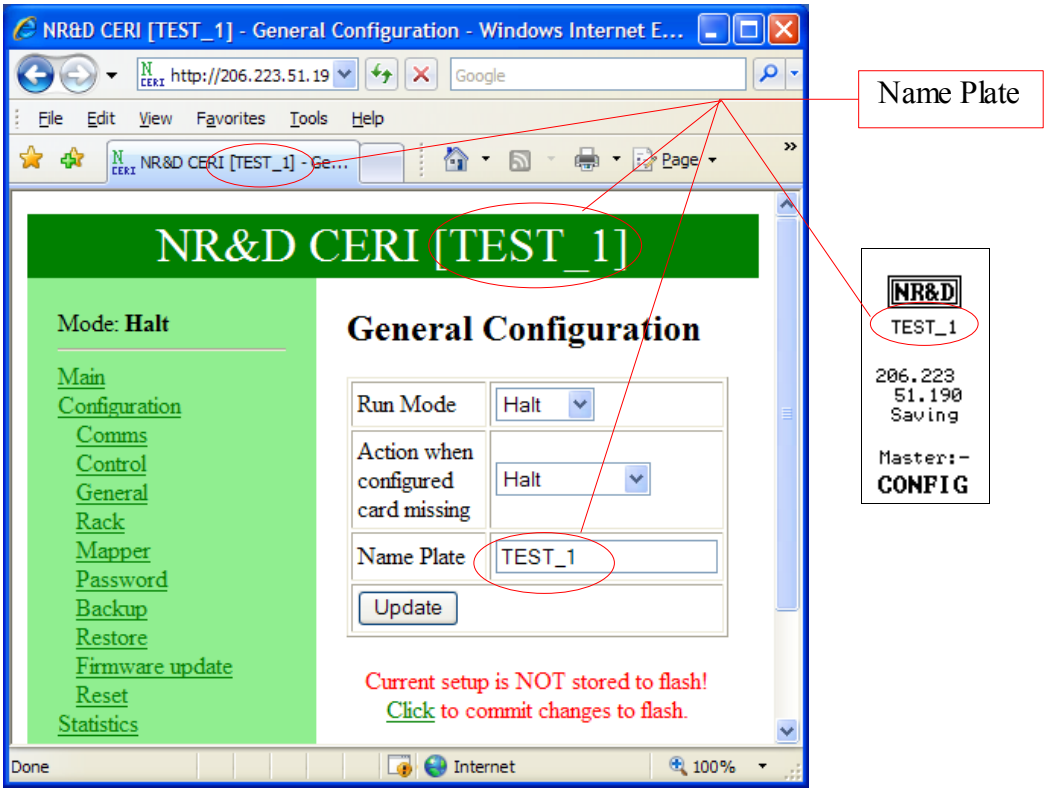


Figure 3.6: General Page

The “Action when configured card missing” determines the action the CERI will take when this event occurs. “Halt” will force the CERI into halt and all outputs to their default state. “Run Allowed” will cause the CERI to post an error but continue to allow the outputs to be remotely controlled.

The “Name Plate” is displayed on the LCD and in the Title of the HTML pages. This value is limited to 16 characters of A-Z, 0-9, and _. All characters will be

capitalized by the CERI. An empty Name Plate will result in the default of CERI to be displayed in the HTML title and front display.

Rack Page

The Rack page is fully described in Chapter 4 on page 37.

Mapper Page

The Mapper page is fully described in Chapter 5 on page 43.

Password Page

The Update Password page allows the changing of the Web page password. This is not the same password used to control access to the front panel of the CERI.

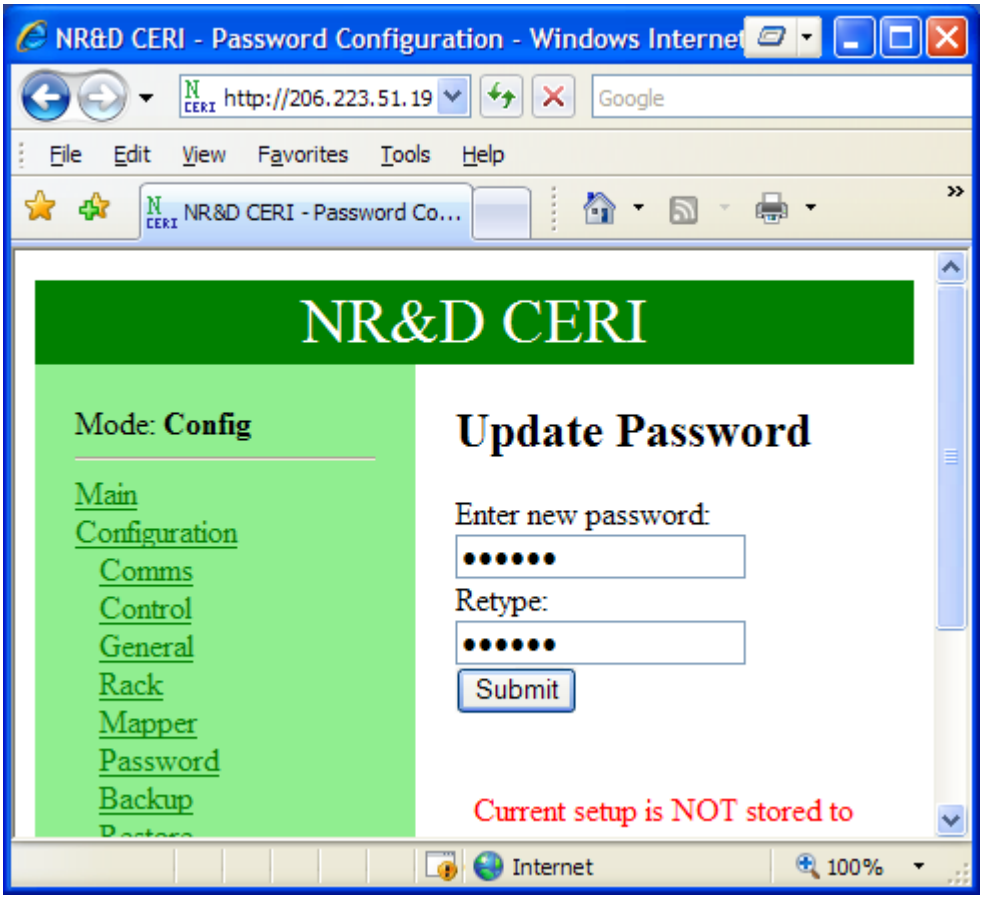


Figure 3.7: Password Update Page

Backup

The Backup page allows the saving of the entire configuration of the CERI to a text file on the PC. Right-click the “here” link and select “Save Target As...” to save a copy of the file. The default filename is config_IPAddress.ceri.

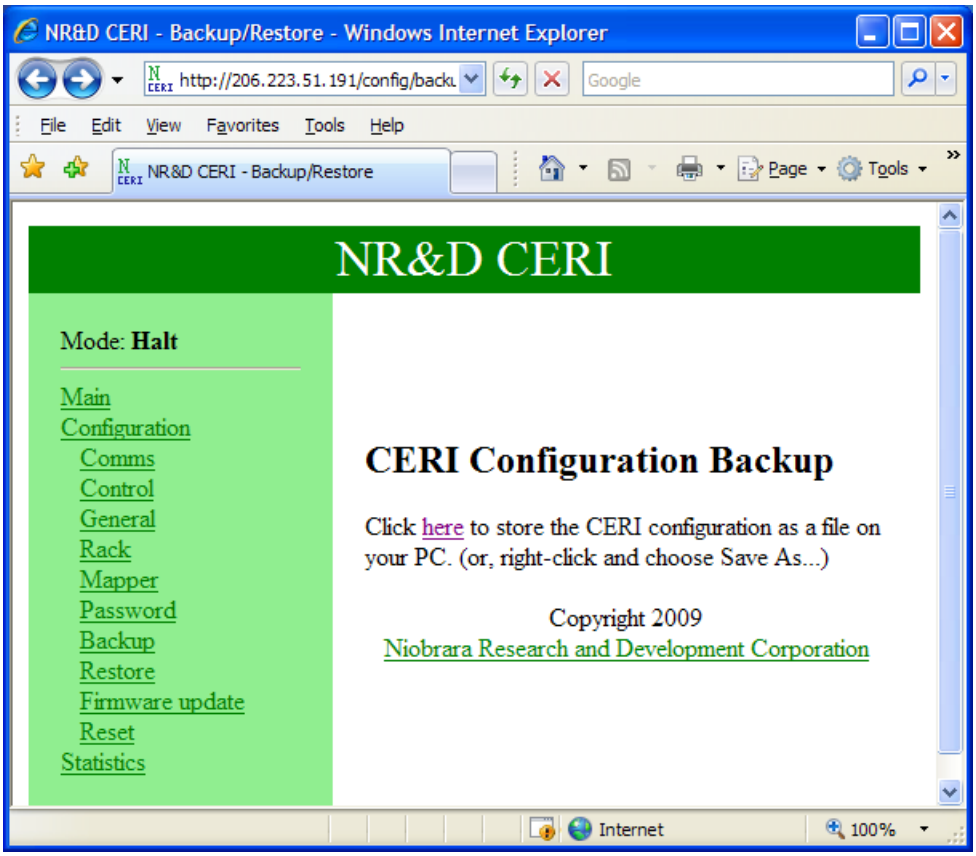


Figure 3.8: Backup Page

The structure of the backup file is simply the register number = value. Values with a leading “x” are in hexadecimal. Factory default values are not included in the backup file to keep the file size down.

Restore Page

The Configuration Restore page simply prompts for the filename of the backup text file. The extension should be .ceri. After selecting the proper file, press “Start Download”. If the process is completed successfully the screen should look like Figure 3.9.

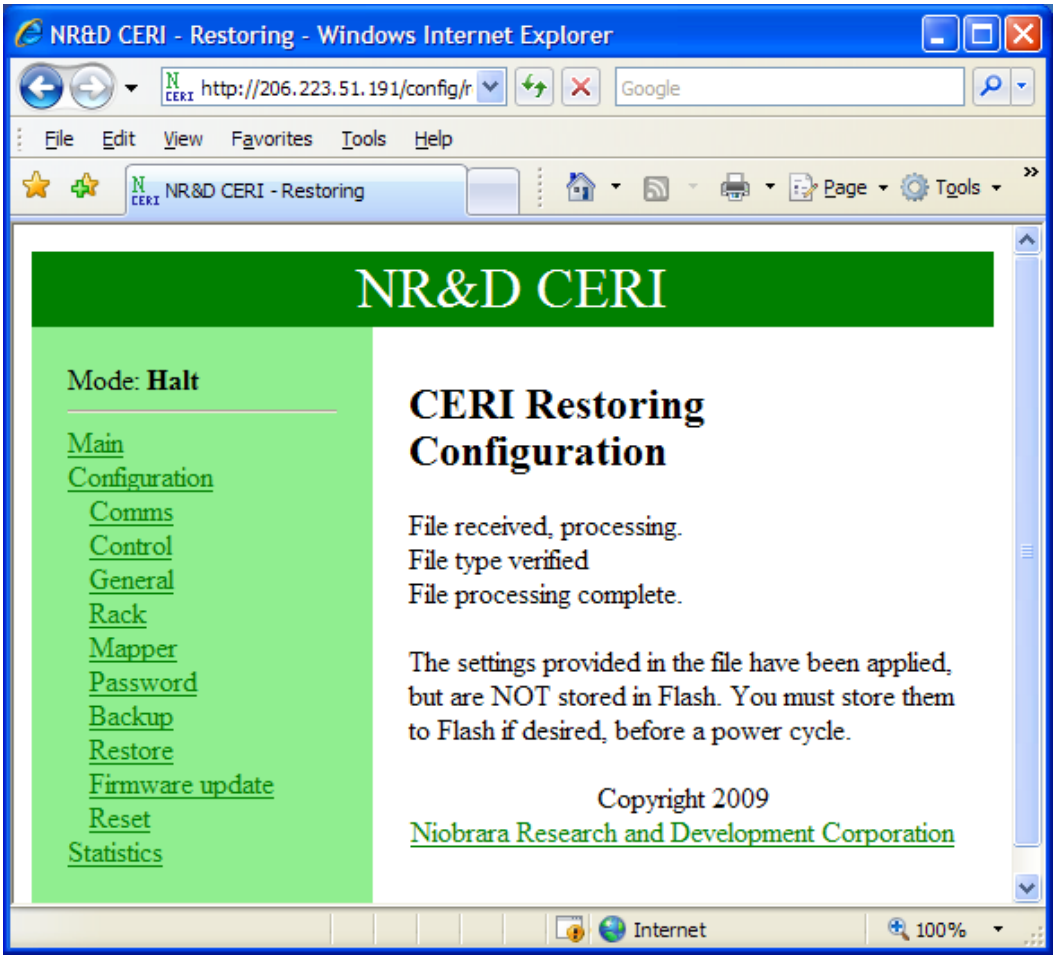


Figure 3.9: Restore

Firmware

The Firmware Upload page allows the easy upgrading of the CERI's firmware over the Ethernet.

NOTE: The CERI must be in Halt to perform this upload.

NOTE: A backup of the CERI should be performed before the firmware update. The new update may cause the CERI to revert to factory defaults. Restoring the old backup will return the CERI to its proper settings.

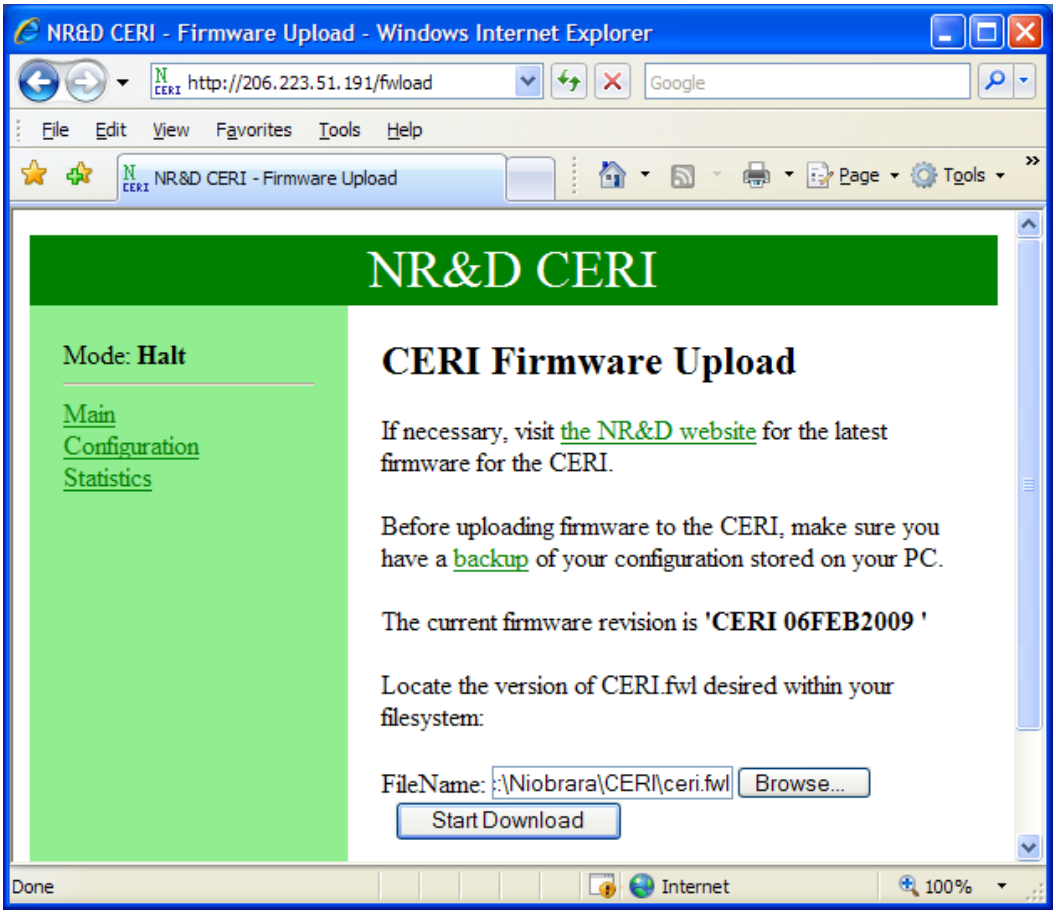


Figure 3.10: Firmware Page

The firmware file is normally saved in c:\Niobrara\ceri\ceri.fwl.

Reset

The Rest page will clear all mapper entries including the Rack and Internal mappers. It will also clear all default output values. It does not affect the configuration stored in Flash memory, only the current working configuration.

To complete the reset, type “YES” in the box and press “Go”.

> NOTE: Reverting the CERI completely to factory defaults may be done through the front panel. See page 99.

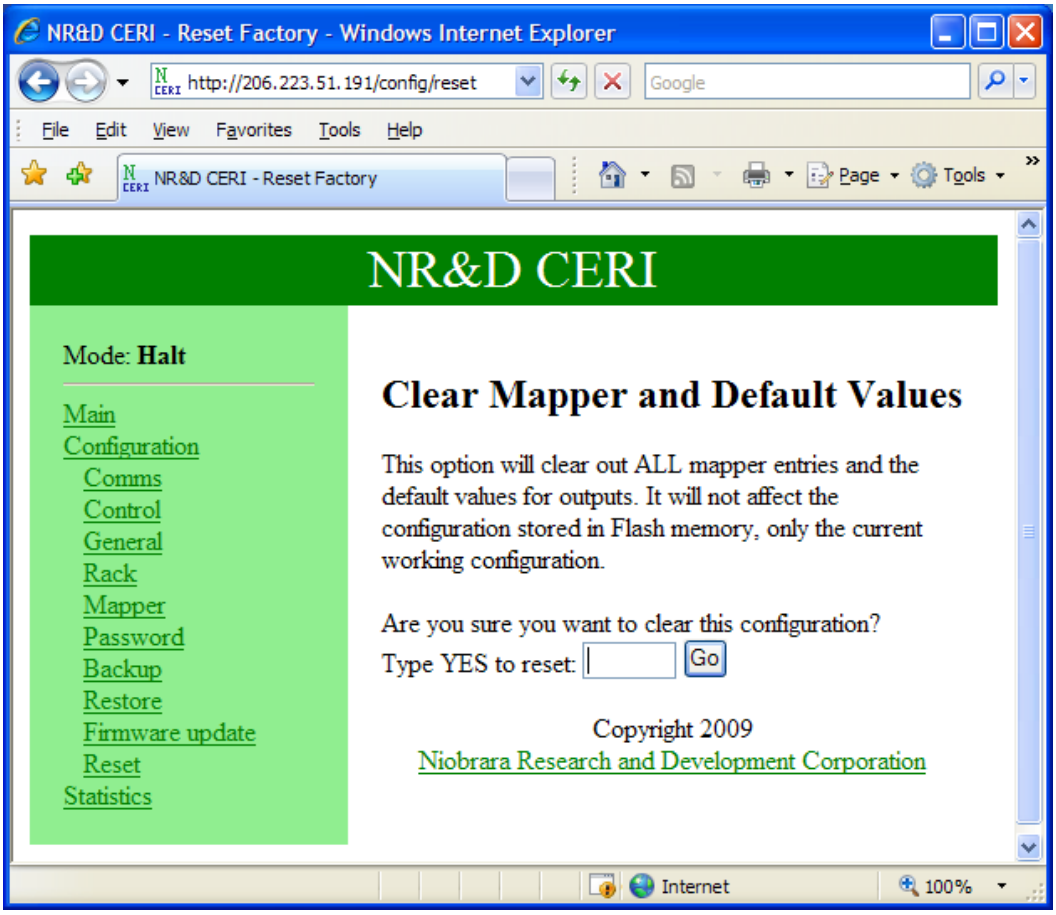


Figure 3.11: Reset Page

Statistics

CERI Statistics

The Statistics page gives a wealth of information about the CERI. This page is automatically refreshed every 30 seconds.

The Firmware and Bootcode Revisions, serial number, MAC Address, scan time, IP Address of the current master, Ethernet and Serial port statistics, and per client statistics are all displayed.

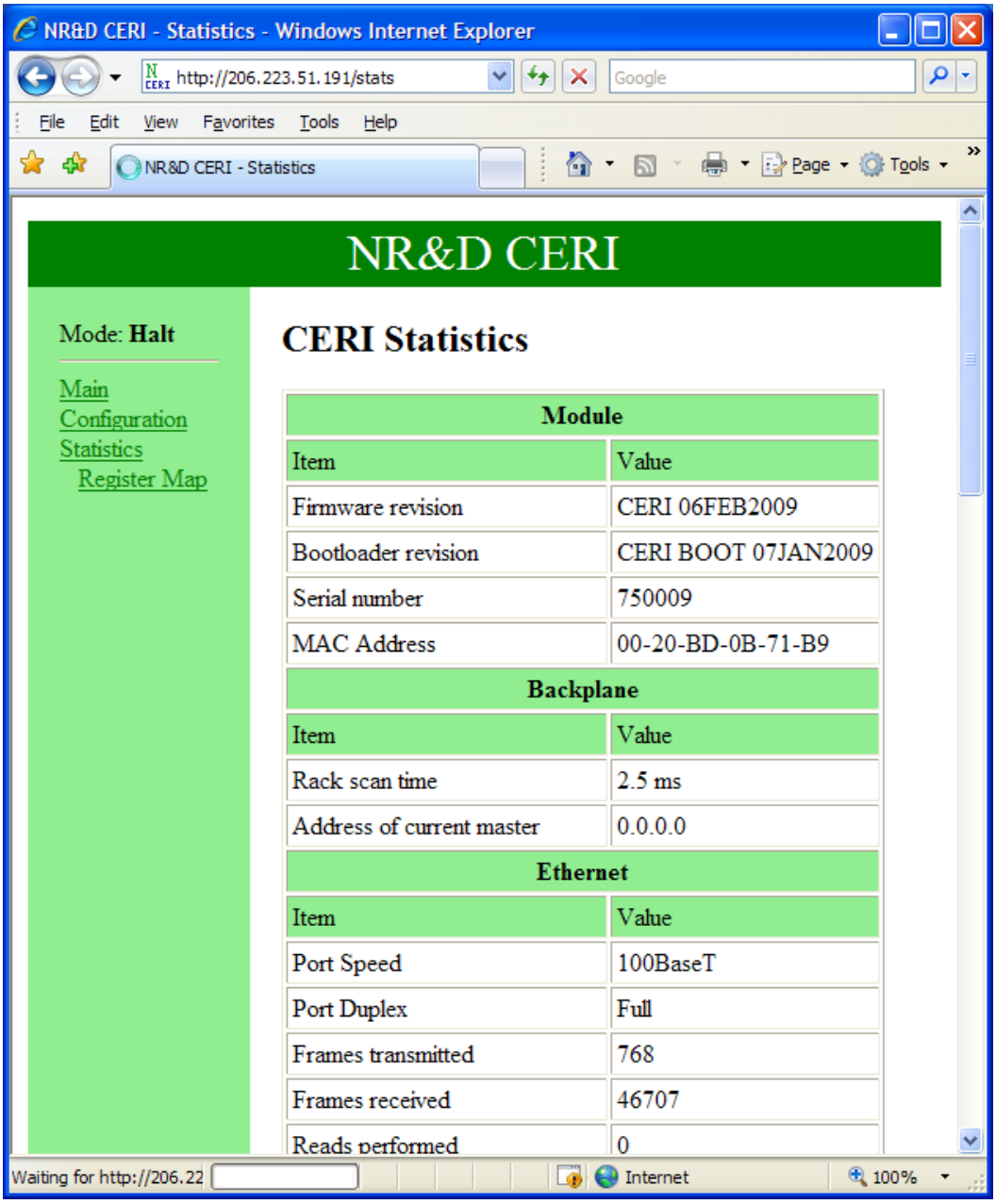


Figure 3.12: Statistics Page

Register Map

The Register Map page gives a cross-reference of all Drop 0/1 registers in use. Source registers (outputs) are shown in black while destination registers (inputs) are shown in blue. Registers used in both the Rack and Internal mapping are shown.

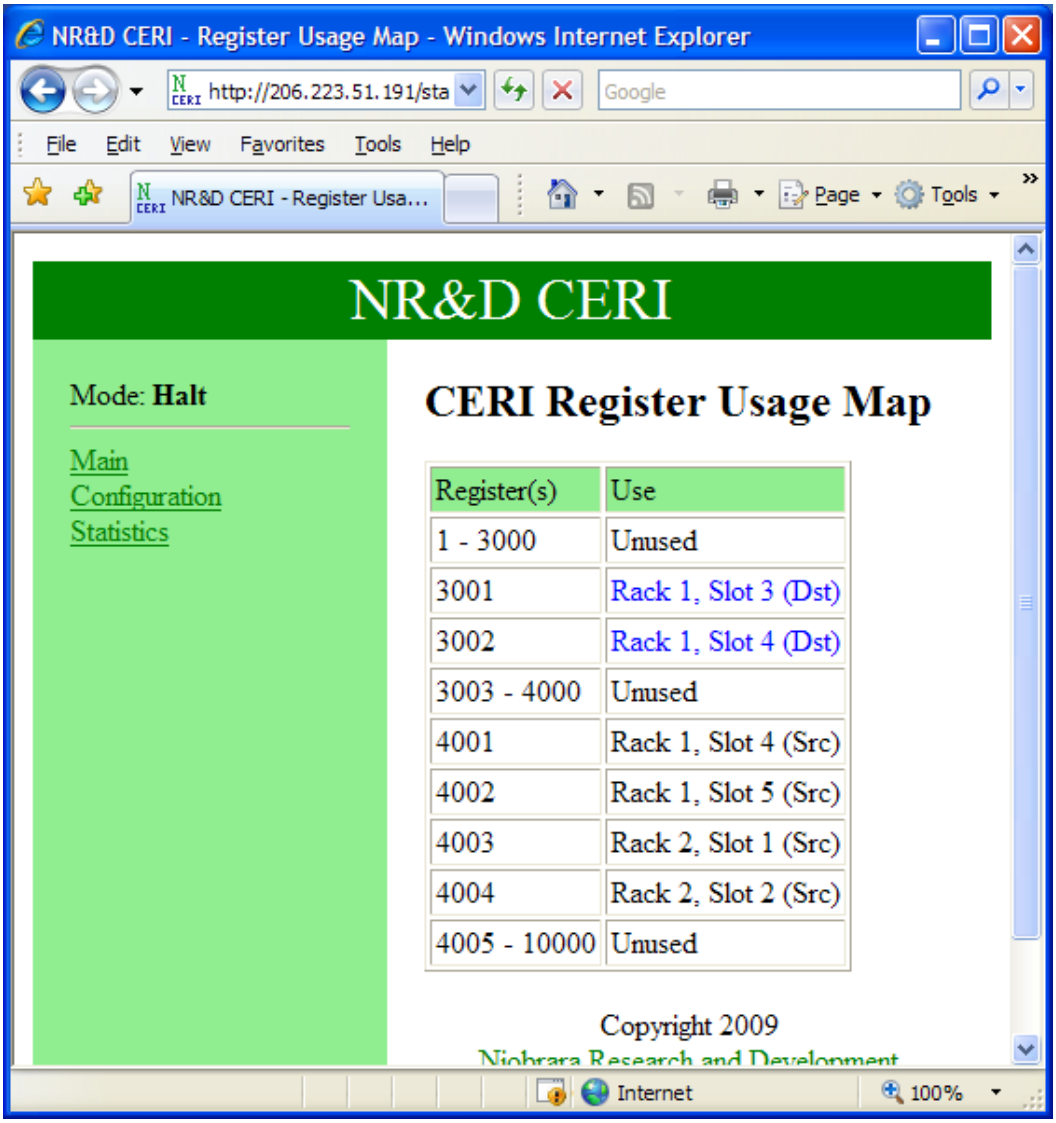


Figure 3.13: Register List

4 Rack

Figure 4.1 shows the features of the Rack I/O Configuration Web page of the CERI.

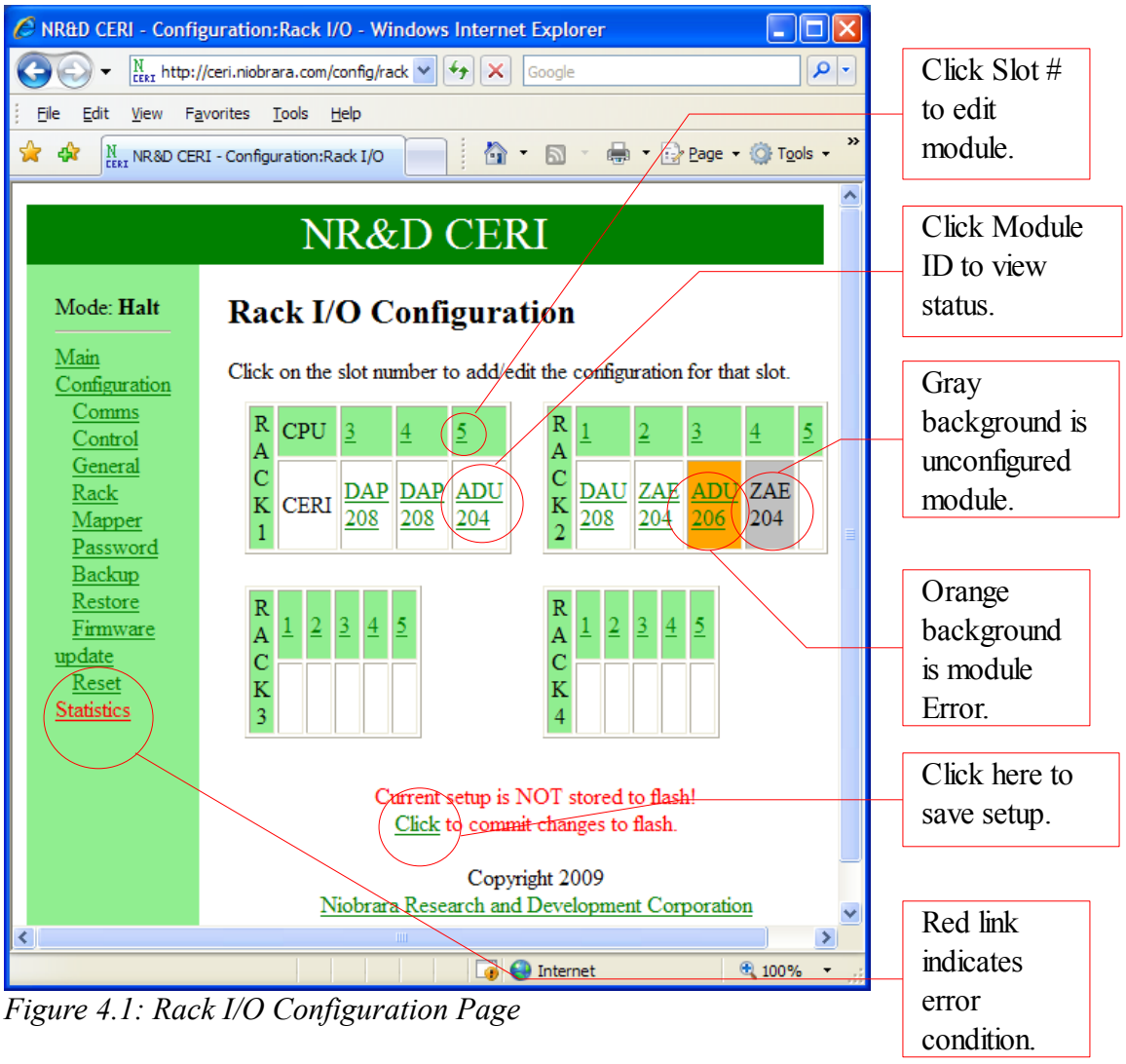


Figure 4.1: Rack I/O Configuration Page

This Web page is accessed by the Configuration>Rack links in the green column.

The layout of the racks on the Web page is always 1-2/3-4 and may not bare resemblance to the actual physical layout of the A120 I/O. The CERI always displays all four racks,

even if they don't physically exist. Unused slots should remain empty in the CERI's configuration.

Detected A120 modules are displayed by name in their slot. If the module is configured in the CERI then this name will also be a link. If a module matches the ID configured in the CERI then the background will be white. If a module is properly configured but reporting a module error or the module ID doesn't match the configuration then the background will be orange. If a module is not yet configured then the background will be gray.

Many A120 cards share the same module ID making it impossible for the CERI to accurately determine which card is present. The CERI will display the detected card name with "*" characters in the digits it is unable to uniquely define until the proper card is selected. Figure 4.2 shows an example of a detected module DAP 2*8. This card may be a DAP 208 or a DAP 258. Both cards share the same module ID and behave the same across the backplane.

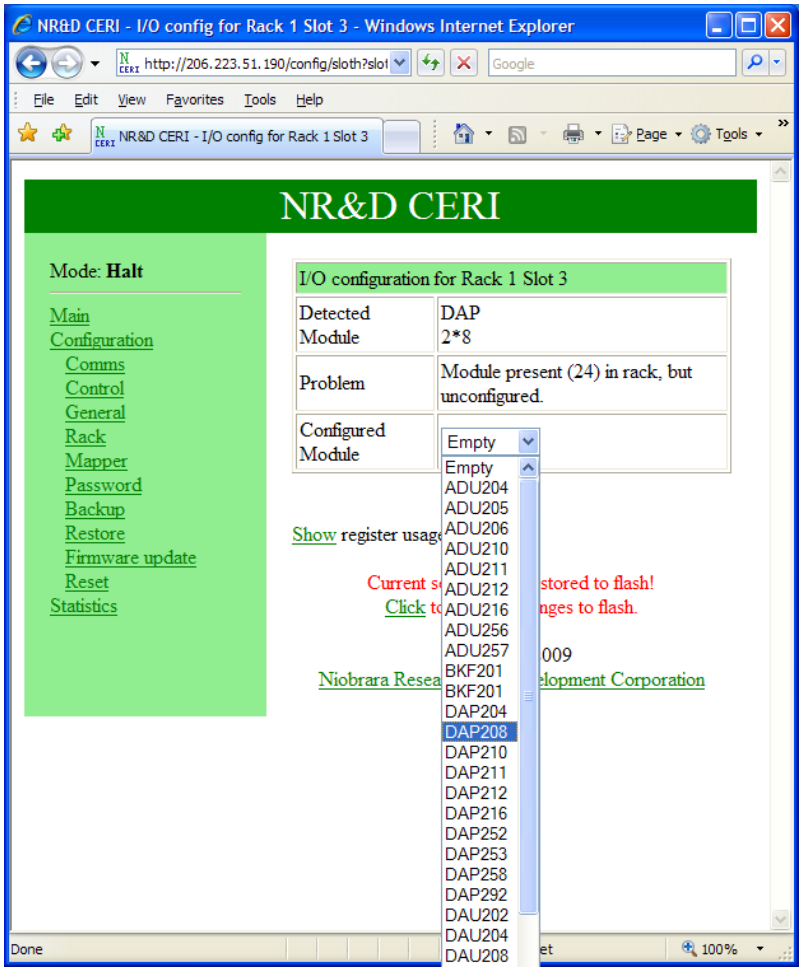


Figure 4.2: Module Selection

A slot is edited by simply clicking on the slot number of the appropriate rack. A page similar to Figure 4.3 will be shown.

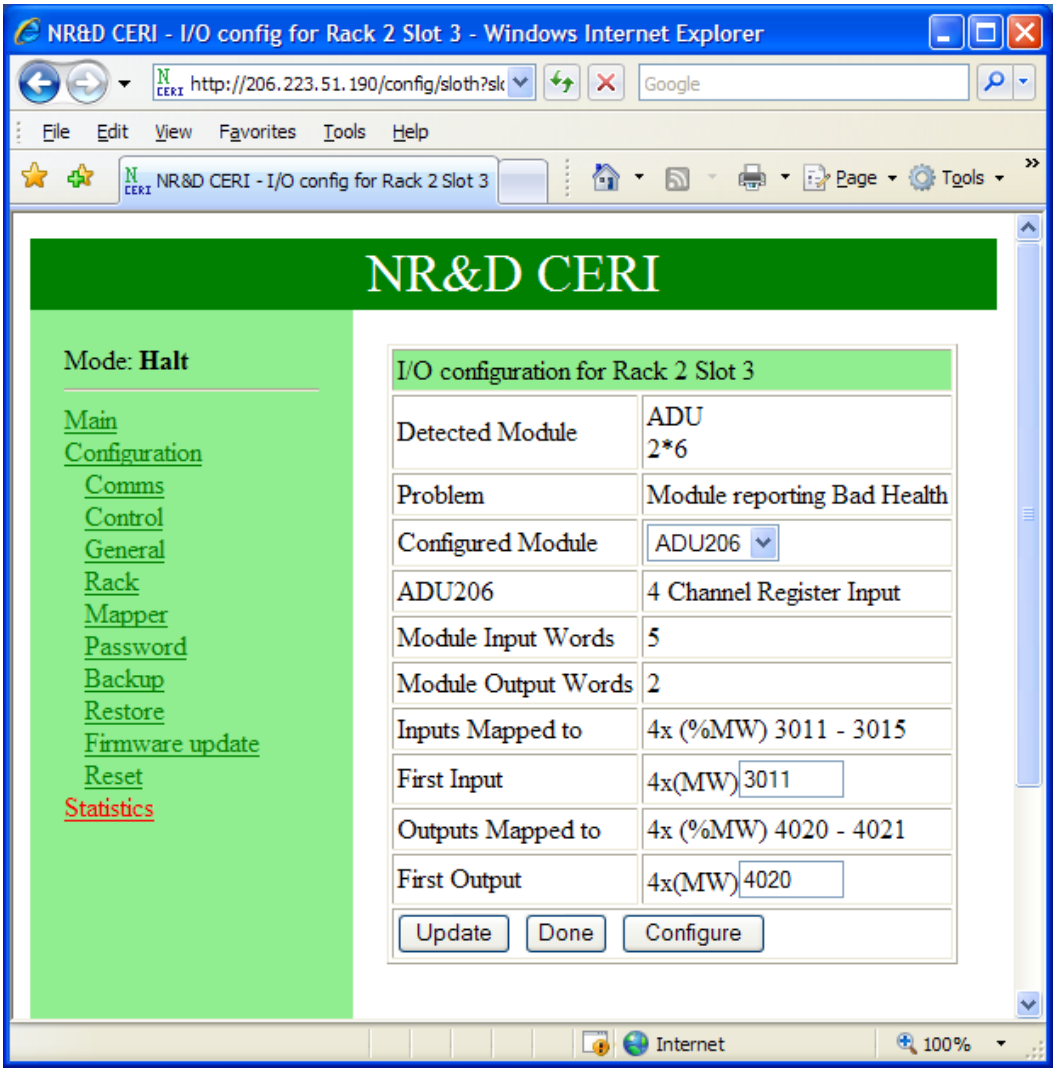


Figure 4.3: Module Edit Page

The First Input value determines where the 5 words of input are placed in the drop 0/1 register area. The First Output determines where the 2 words of output start.

The ADU 206 includes a "Configure" button used to set up the analog inputs (Figure 4.4). In most cases that include a "Configure" button, most if not all of the output words assigned to that card are set through the Web page and do not need to be controlled from the Master.

> **Recommended Practice**: Niobrara recommends that analog input cards have their outputs mapped to registers not written by the controlling PLC master. These outputs are usually configured once through the CERI's web page and should not be written by the PLC.

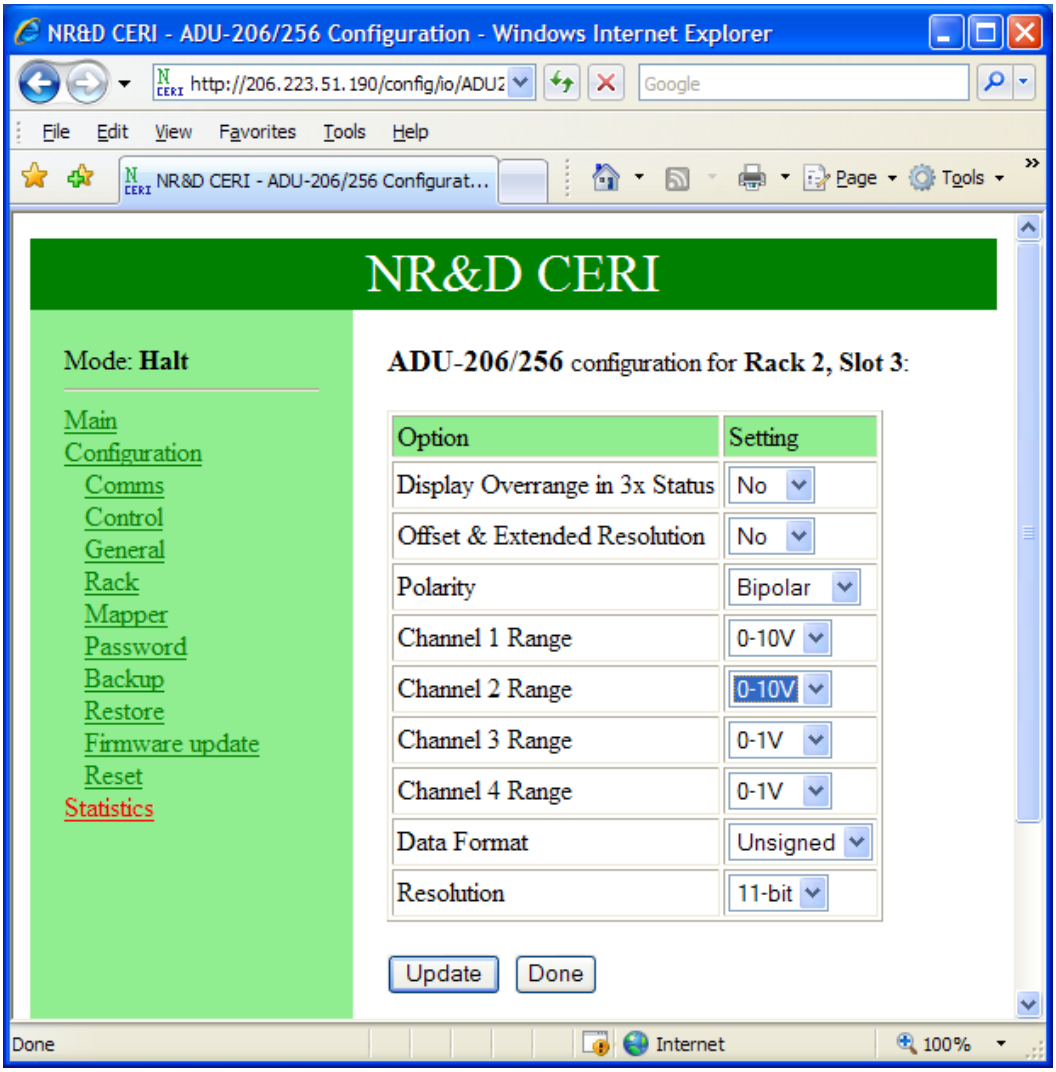


Figure 4.4: Configure Page for ADU 206

Clicking on the Module ID on the Rack page will give a status page for that card (Figure 4.5). This page gives a summary about the configuration as well as the actual data reported by the card.

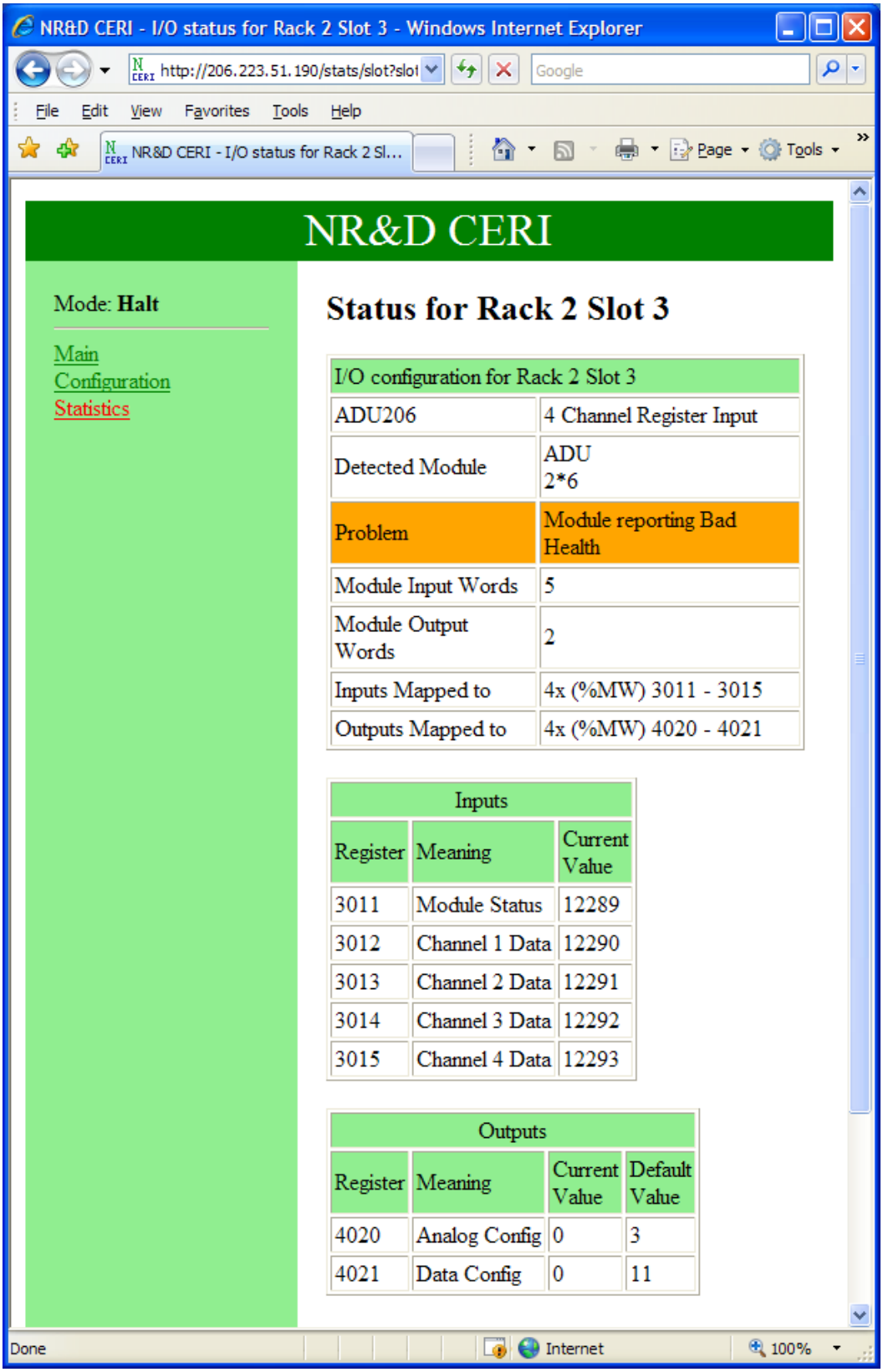


Figure 4.5: Status Page for ADU 206

5 Mapper

This chapter explores the Internal Mapper feature in detail.

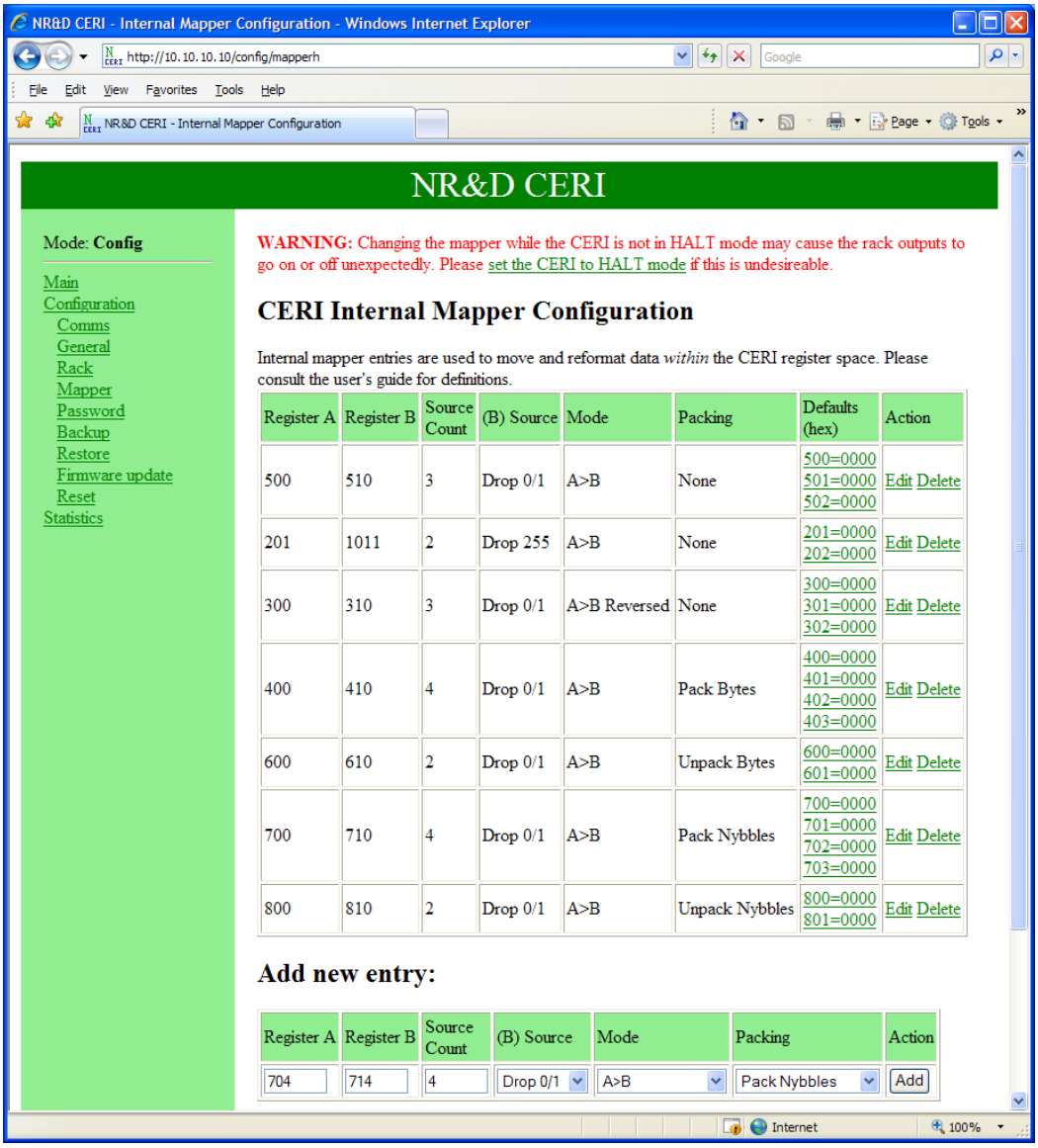


Figure 5.1: Internal Mapper Example Web Page

The CERI can support up to 50 entries in its mapping machine (See Drop 255 Register List on page 102). These 50 entries are shared between the Rack Map entries and the Internal Map entries. There are 18 possible A120 Rack entries which means there are a minimum of 32 Internal Map entries available for use.

Mapper Description

- Register A – This value is the starting register in the Drop 0/1 data space for this mapper entry. The valid range is 1 through 10000.
- Register B – This value is the starting register in either the Drop 0/1 data space or the Drop 255 data space. The valid rage is 1 through 40000.
- Source Count – This value determines the number of registers moved, packed, or unpacked in this operation. The valid rage is 1 through 255.
- Mode – There are four choices for the Mode:
    - A>B – The value from Register A is moved to Register B. The Source Count and Packing settings determine how many other values are also moved.
    - B<A – The value from Register B is moved to Register A. The Source Count and Packing settings determine how many other values are also moved.
    - A>B Reversed – The value from Register A is moved to Register B with all of the bits reversed. This means that the value of bit 0 (lsb) of "A" is now bit 15 (msb) of "B". Bit 1 of "A" is now bit 14 of "B" and so on.
    - B<A Reversed – The value from Register B is moved to Register A with all of the bits reversed.
- Packing – There are four choices for Packing:
    - None – The data is transferred directly as indicated by the Mode setting.
    - Pack Bytes – The data from the least significant bytes of the source register and source + 1 are compressed into the target register. The source count must be an even number (2, 4, 6, etc.). Pack bytes is typically used with 8-bit input cards when aligning the bit numbers to 1x inputs.
    - Unpack Bytes – The data from the source register is split so the most significant byte of the source is loaded into the least significant byte of the target and the least significant byte of the source is loaded into the least significant byte of the target + 1. Unpack Bytes is typically used with 8-bit output cards when aligning the bit numbers to 0x coils.
    - Pack Nybbles – The data from the least significant nybble of the

source register and places this value into the most significant nybble of the target register. Additionally, it places the least significant nybble of the source + 1 register and places this value into the next to least significant nybble of the target register. The Source Count must be an even number (2, 4, 6, etc.). Pack Nybbles would be used with 4-bit input cards.

- Unpack Nybbles – The most significant nybble from the source register is placed into the least significant nybble of the target register. Additionally, the next to least significant nybble of the source register is placed into the least significant nybble of the target + 1 register. Unpack Nybbles is typically used with 4-bit output cards when aligning the bit numbers to 0x coils.

Mapper Examples

These examples make no notice of the Default settings and are just concerned with showing how the map entries function.

A>B Copy

This example is a simple copy of data from registers 500, 501, and 502 to registers 510, 511, and 512.

Table 5.1: Mapper A>B Copy

Register A	Register B	Source Count	(B) Source	Mode	Packing
500	510	3	Drop 0	A>B	None

Table 5.2: Mapper A>B Copy

Source Register	Value (hex)		Target Register	Value (hex)
500	1234	→	510	1234
501	5678	→	511	5678
502	ABCD	→	512	ABCD

B<A Drop 255 Copy

The example below copies the “Status Register” and “Scan Time” of the CERI in drop 255 registers 1011 and 1012 to data registers 201 and 202 in drop 0.

Table 5.3: Mapper B<A Drop 255 Copy

Register A	Register B	Source Count	(B) Source	Mode	Packing
201	1011	2	Drop 255	B>A	None

Table 5.4: Mapper Drop 255 Copy

Source Register	Drop	Value (decimal)		Target Register	Drop	Value (decimal)
1011	255	4	→	201	0	4
1012	255	51	→	202	0	51

The value 4 indicates the CERI is running and the 51 indicates a scan time of 5.1mS.

A>B Reversed

This example is a copy of data from registers 300, 301, and 302 to 310, 311, and 312 while reversing the bit order.

Table 5.5: Mapper A>B Reversed

Register A	Register B	Source Count	(B) Source	Mode	Packing
300	310	3	Drop 0	A>B Reversed	None

Table 5.6: Mapper A>B Reversed

Source Register	Value (hex)	Value (binary)		Target Register	Value (hex)	Value (binary)
300	1234	0001 0010 0011 0100	→	310	2C48	0010 1100 0100 1000
301	4000	0100 0000 0000 0000	→	311	0002	0000 0000 0000 0010
302	0001	0000 0000 0000 0001	→	312	8000	1000 0000 0000 0000

Pack Bytes A>B

Pack Bytes takes the Least Significant Bytes from adjacent registers and packs them into a single registers. The count determines the number of register pairs to pack. The Most Significant Byte of each source register is ignored.

This example is a pack of the LSB data from registers 400 and 401 into 410 and

from 402 and 403 into 411.

Table 5.7: Mapper Pack Bytes

Register A	Register B	Source Count	(B) Source	Mode	Packing
400	410	4	Drop 0	A>B	Pack Bytes

Table 5.8: Mapper Pack Bytes

Source Register	Value (hex)		Target Register	Value (hex)
400	1234	→	410	3478
401	5678	→		
402	9ABC	→	411	BCF0
403	DEF0	→		

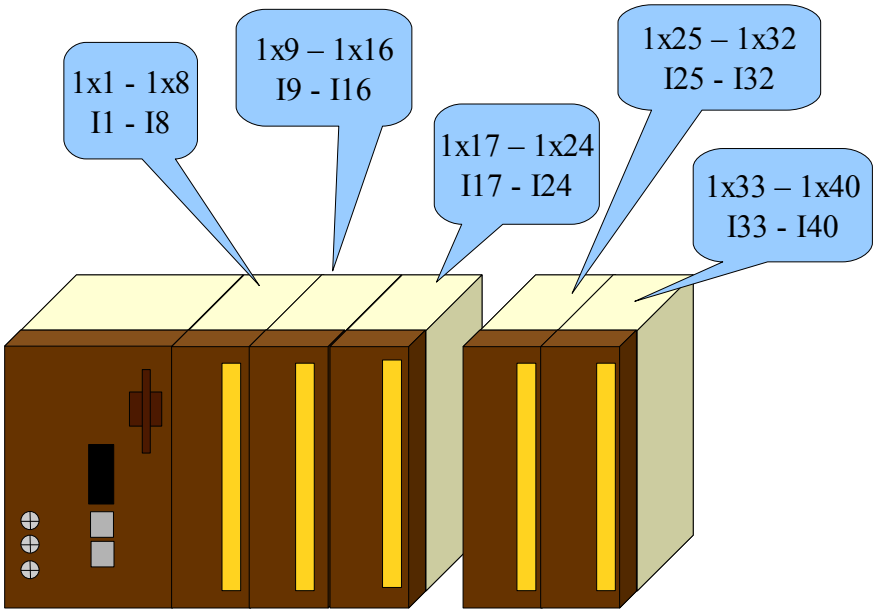
The Pack Bytes mapper is used to compress 8-bit discrete input cards into the same bit order used by the original PLC.

Figure 5.2 shows a Compact PLC with 5 DEP-208 8-bit input cards. Each card is traffic-copped for 8 bits. Table 5.9 shows the PLC memory map.

Table 5.9: DEP-208 Original PLC Traffic Cop

Rack 1						Rack 2			
Slot 3		Slot 4		Slot 5		Slot 1		Slot 2	
Bit	Input	Bit	Input	Bit	Input	Bit	Input	Bit	Input
1x1	I1	1x9	I9	1x17	I17	1x25	I25	1x33	I33
1x2	I2	1x10	I10	1x18	I18	1x26	I26	1x34	I34
1x3	I3	1x11	I11	1x19	I19	1x27	I27	1x35	I35
1x4	I4	1x12	I12	1x20	I20	1x28	I28	1x36	I36
1x5	I5	1x13	I13	1x21	I21	1x29	I29	1x37	I37
1x6	I6	1x14	I14	1x22	I22	1x30	I30	1x38	I38
1x7	I7	1x15	I15	1x23	I23	1x31	I31	1x39	I39
1x8	I8	1x16	I16	1x24	I24	1x32	I32	1x40	I40

Figure 5.2 DEP-208 8-bit Input Cards



It would be convenient for the CERI to provide a mapping of the input data to simply allow an I/O Scanner read from the new PLC to reproduce the original mapping.

Table 5.10 shows a typical mapping of a CERI with five DEP-208 cards assigned to registers 101 through 106. If the PLC did an I/O Scan read of these 6 words, the data would end up with 8-bit gaps and the number would not align with the old system.

Table 5.10: I/O Data from normal CERI DEP-208 configuration

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0101									1	2	3	4	5	6	7	8
									R1	R2	R3	R4	R5	R6	R7	R8
4x0102									9	10	11	12	13	14	15	16
									R9	R10	R11	R12	R13	R14	R15	R16
4x0103									17	18	19	20	21	22	23	24
									R17	R18	R19	R20	R21	R22	R23	R24
4x0104									25	26	27	28	29	30	31	32
									R25	R26	R27	R28	R29	R30	R31	R32
4x0105									33	34	35	36	37	38	39	40
									R33	R34	R35	R36	R37	R38	R39	R40
4x0106									41	42	43	44	45	46	47	48
									R41	R42	R43	R44	R45	R46	R47	R48

Adding the mapper entry in Table 5.11 to the CERI results in the data being placed in registers 111 through 113 as shown in Table 5.12.

Table 5.11: Mapper Pack Bytes

Register A	Register B	Source Count	(B) Source	Mode	Packing
101	111	6	Drop 0	A>B	Pack Bytes

Table 5.12: I/O Data to be read with I/O Scanner after Pack Bytes Mapper

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0111	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
4x0112	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26	R27	R28	R29	R30	R31	R32
4x0113	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
	R33	R34	R35	R36	R37	R38	R39	R40	R41	R42	R43	R44	R45	R46	R47	R48

An I/O Scanner entry that would be used to read this input data from a CERI would look something like Table 5.13. The data that would show up in the PLC in the same order as the original system.

Table 5.13: I/O Scanner settings to read the DEP-208 data

Read From	Read To	Read Count
4x00111	1x00001	3

Unpack Bytes A>B

The Unpack Bytes mapper splits the Most Significant Byte (MSB) of the source register and places that data into the Least Significant Byte (LSB) of the target register. It also takes the LSB of the source register and places that data into the LSB of the target register plus 1. The MSB of each target register is zeroed. The count determines the number of source registers to unpack.

This example is a unpack of the MSB data from register 600 into the LSB of 610 and the LSB from 600 into the LSB of 611. This entry also copies the MSB from 601 into the LSB of 612 and the LSB from 601 into the LSB of 613.

Table 5.14: Mapper Unpack Bytes

Register A	Register B	Source Count	(B) Source	Mode	Packing
600	610	2	Drop 0	A>B	Unpack Bytes

Table 5.15: Mapper Unpack Bytes

Source Register	Value (hex)		Target Register	Value (hex)
600	1234		610	0012
			611	0034
601	5678		612	0056
			613	0078

Unpack Bytes is used with 8-bit output cards. Figure 5.3 shows a Compact PLC with 5 DAP-208 8-bit relay output cards. Each card is traffic-copped for 8 bits. Table 5.17 shows the PLC memory map.

An I/O Scanner entry that would be used to push this output data to a CERI would look something like Table 5.16. The data that would show up in the CER is described in Table 5.18.

Table 5.16: I/O Scanner settings to push the DAP-208 data

Write From	Write To	Write Count
0x00001	4x00101	3

Table 5.17: DAP-208 Example

Rack 1						Rack 2			
Slot 3		Slot 4		Slot 5		Slot 1		Slot 2	
Coil	Relay	Coil	Relay	Coil	Relay	Coil	Relay	Coil	Relay
0x1	R1	0x9	R9	0x17	R17	0x25	R25	0x33	R33
0x2	R2	0x10	R10	0x18	R18	0x26	R26	0x34	R34
0x3	R3	0x11	R11	0x19	R19	0x27	R27	0x35	R35
0x4	R4	0x12	R12	0x20	R20	0x28	R28	0x36	R36
0x5	R5	0x13	R13	0x21	R21	0x29	R29	0x37	R37
0x6	R6	0x14	R14	0x22	R22	0x30	R30	0x38	R38
0x7	R7	0x15	R15	0x23	R23	0x31	R31	0x39	R39
0x8	R8	0x16	R16	0x24	R24	0x32	R32	0x40	R40

Figure 5.3 DAP-208 8-bit Relay Cards

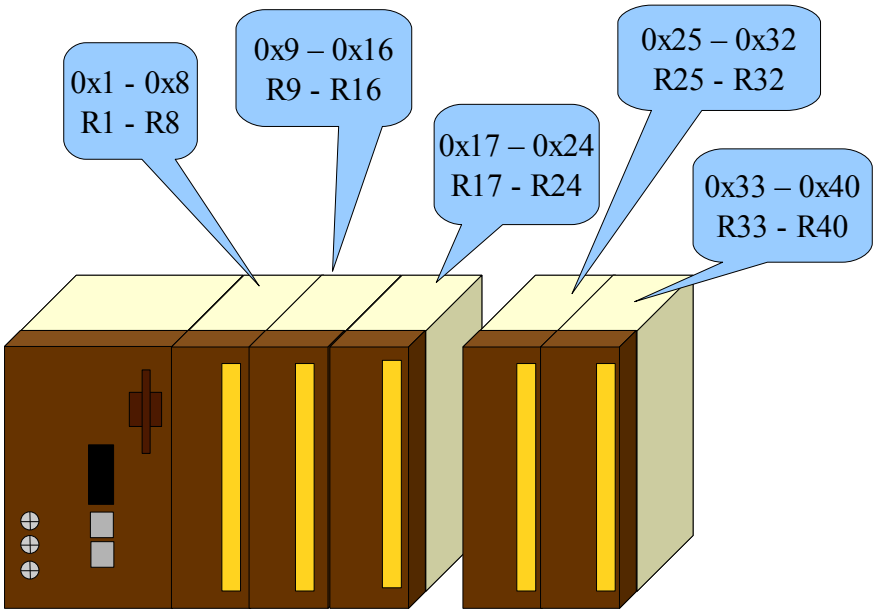


Table 5.18: I/O Data pushed from I/O Scanner

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0101	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
4x0102	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26	R27	R28	R29	R30	R31	R32
4x0103	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
	R33	R34	R35	R36	R37	R38	R39	R40	R41	R42	R43	R44	R45	R46	R47	R48

Now add the mapper entry in Table 5.19 to the CERI and the new data is placed in registers 111 through 116 as shown in Table 5.20.

Table 5.19: Mapper Unpack Bytes

Register A	Register B	Source Count	(B) Source	Mode	Packing
101	111	3	Drop 0	A>B	Unpack Bytes

Table 5.20: I/O Data after mapper byte unpack

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0111									1	2	3	4	5	6	7	8
									R1	R2	R3	R4	R5	R6	R7	R8
4x0112									9	10	11	12	13	14	15	16
									R9	R10	R11	R12	R13	R14	R15	R16
4x0113									17	18	19	20	21	22	23	24
									R17	R18	R19	R20	R21	R22	R23	R24
4x0114									25	26	27	28	29	30	31	32
									R25	R26	R27	R28	R29	R30	R31	R32
4x0115									33	34	35	36	37	38	39	40
									R33	R34	R35	R36	R37	R38	R39	R40
4x0116									41	42	43	44	45	46	47	48
									R41	R42	R43	R44	R45	R46	R47	R48

The resulting data is now in the proper order for the CERI to use with a DAP-208

module. Now, it is simply required to configure each relay card in the CERI to be assigned to registers 111 through 116.

Pack Nybbles A>B

The Pack Nybbles mapper takes the Least Significant Nybble (LSN) of the source register and places that data into the Most Significant Nybble (MSN) of the target register. It then takes the LSN of the source register+1 and places that data into the upper nybble of the LSB of the target register. All other bits in the target register are zeroed. The count determines the number of source registers to compress.

This example is a pack of the LSN data from register 700 and the LSN from register 701 into register 710 and the LSN from registers 702 and 703 into register 711.

Table 5.21: Mapper Pack Nybbles

Register A	Register B	Source Count	(B) Source	Mode	Packing
700	710	4	Drop 0	A>B	Pack Nybbles

Table 5.22: Internal Mapper Pack Bytes

Source Register	Value (hex)		Target Register	Value (hex)
700	1234		710	4080
701	5678			
702	9ABC		711	C010
703	DEF1			

Pack Nybbles would be used with a 4-bit input card, but there are no know 4-bit input A120 cards so no example will be shown.

Unpack Nybbles A>B

This example is a unpack of the most significant nybble (MSN) data from register 800 into the LSN of 810 and the next to LSN from 800 into the LSN of 811. This entry also copies the MSN from 801 into the LSN of 812 and the next to LSN from 801 into the LSN of 813.

Table 5.23: Mapper Unpack Nybbles

Register A	Register B	Source Count	(B) Source	Mode	Packing
800	810	2	Drop 0	A>B	Unpack Nybbles

Table 5.24: Mapper Unpack Nybbles

Source Register	Value (hex)		Target Register	Value (hex)
800	1234		810	0001
			811	0003
801	5678		812	0005
			813	0007

Unpack Nybbles is used with 4-bit output cards. Figure 5.4 shows a Compact PLC with 5 DAP-204 4-bit relay output cards. Each card is traffic-copped for 8 bits. Table 5.26 shows the PLC memory map. Notice that each card only uses the first four bits assigned to the slot.

An I/O Scanner entry that would be used to push this output data to a CERI would look something like Table 5.25. The data that would show up in the CER is described in Table 5.27.

Table 5.25: I/O Scanner settings to push the DAP-204 data

Write From	Write To	Write Count
0x00001	4x00101	3

Table 5.26: DAP-204 Example

Rack 1						Rack 2			
Slot 3		Slot 4		Slot 5		Slot 1		Slot 2	
Coil	Relay	Coil	Relay	Coil	Relay	Coil	Relay	Coil	Relay
0x1	R1	0x9	R5	0x17	R9	0x25	R13	0x33	R17
0x2	R2	0x10	R6	0x18	R10	0x26	R14	0x34	R18
0x3	R3	0x11	R7	0x19	R11	0x27	R15	0x35	R19
0x4	R4	0x12	R8	0x20	R12	0x28	R16	0x36	R20
0x5		0x13		0x21		0x29		0x37	
0x6		0x14		0x22		0x30		0x38	
0x7		0x15		0x23		0x31		0x39	
0x8		0x16		0x24		0x32		0x40	

Figure 5.4 DAP-204 4-bit Relay Cards

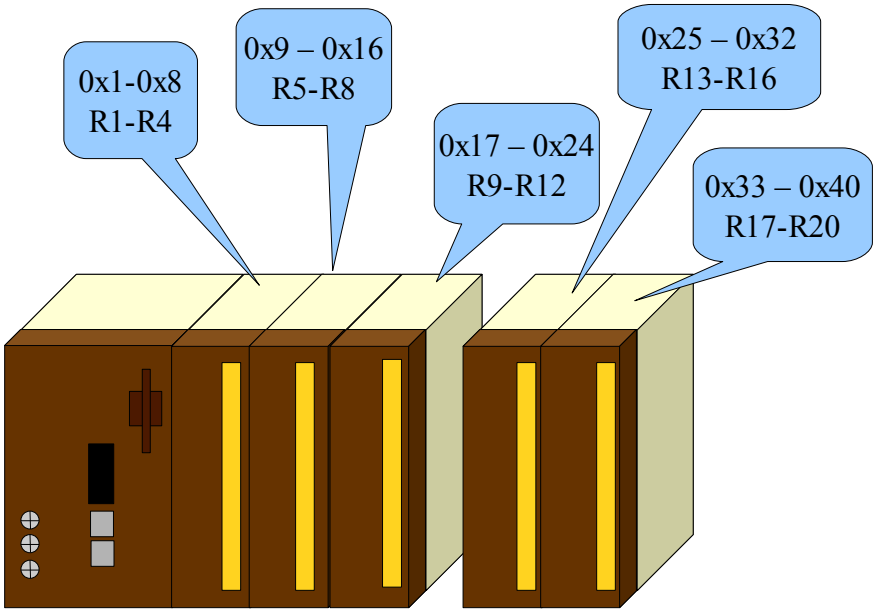


Table 5.27: I/O Data pushed from I/O Scanner

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0101	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	R1	R2	R3	R4					R5	R6	R7	R8				
4x0102	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	R9	R10	R11	R12					R13	R14	R15	R16				
4x0103	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
	R17	R18	R19	R20												

Now add the mapper entry in Table 5.28 to the CERI and the new data is placed in registers 111 through 116 as shown in Table 5.29.

Table 5.28: Mapper Unpack Nybbles

Register A	**Register B**	**Source Count**	**(B) Source**	**Mode**	**Packing**
101	111	3	Drop 0	A>B	Unpack Nybbles

Table 5.29: I/O Data after mapper nybble unpack

	Bit Number															
CERI Register	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4x0111													1	2	3	4
													R1	R2	R3	R4
4x0112													9	10	11	12
													R5	R6	R7	R8
4x0113													17	18	19	20
													R9	R10	R11	R12
4x0114													25	26	27	28
													R13	R14	R15	R16
4x0115													33	34	35	36
													R17	R18	R19	R20
4x0116													41	42	43	44

The resulting data is now in the proper order for the CERI to use with a DAP-204

module. Now, it is simply required to configure each relay card in the CERI to be assigned to registers 111 through 115.

Note that register 116 is reserved for PLC bits 41 through 44 and should not be used elsewhere within the CERI.

6 A120 I/O

The default operation of many A120 I/O cards with the CERI is the same as the operation of the card configured for 3x-register operation using Concept. Many of the intelligent cards require the CERI to perform automatic multiplexing/demultiplexing of the data across the backplane so these cards will have many more input and output registers than normally traffic-copped with a Compact PLC. The register maps for each supported module is shown in this chapter.

> NOTE: For complete module wiring and operating information consult the Modicon A120 Series I/O Modules User Guide (890 USE 109 00).

ADU 204 (4-point Voltage/RTD Analog Input)

Modicon Module ID: x20 (32), NRD Module ID: x14 (20)

The ADU 204 uses four 4x-registers (In-0 through In-3) for the analog data from Channels 1 through 4. There are no output registers assigned to this card.

Table 6.1: ADU 204 input register map

4x Register	Description
In-0	Channel 1 input value
In-1	Channel 2 input value
In-2	Channel 3 input value
In-3	Channel 4 input value

ADU 205 (4-point Voltage/Current Analog Input)

Modicon Module ID: x22 (34), NRD Module ID: x15 (21)

The ADU 205 uses four 4x-register inputs (In-0 through In-3) and five 4x-register outputs (Out-0 through Out-4). The input registers show the analog values for Channels 1 through 4 while the output registers set the resolution and Channel configuration.

> **NOTE**: The values used in the four output registers are typically set through the Configuration page on the CERI's Web server. These values will not change

during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.2: ADU 205 input register map

4x Register	Description
In-0	Channel 1 input value
In-1	Channel 2 input value
In-2	Channel 3 input value
In-3	Channel 4 input value

Table 6.3: ADU 205 output register map

4x Register	Description
Out-0 (Resolution)	(Module Resolution Configuration in hex) 0C = 12 bit 0E = 12 bit + sign 0B = 13 bit 0F = 15 bit + sign 0D = 16 bit
Out-1 (Channel 1)	(Configuration Values in hex) 00 = Inactive 01 = -20V to +20V 02 = -40mA to +40mA 04 = -10V to +10V 08 = -20mA to +20mA 10 = 0mA to 20mA 20 = 4mA to 20mA 40 = 0V to 10V 80 = 0V to 20V
Out-2 (Channel 2)	(Same Configuration Values as above)
Out-3 (Channel 3)	(Same Configuration Values as above)
Out-4 (Channel 4)	(Same Configuration Values as above)

ADU 206 (4-point Voltage/Current Isolated Analog Input)

Modicon Module ID: x23 (35), NRD Module ID: x16 (22)

The ADU 206 use five 4x-register inputs (In-0 through In-4) and two 4x-register outputs (Out-0 and Out-1). The input registers show the status and analog values for Channels 1 through 4 while the output registers set the resolution and Channel configuration.

> **NOTE**: The values used in the two output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.4: ADU 206 input register map

4x Register	Description
In-0 (Status)	Bitmap (bit 0 is LSB) bits 8-15 not used bit 7 = set on Fault bit 6 = set if external supply bad bit 5 = Offset and extended resolution turned on bit 4 = set if Unipolar, clear if Bipolar bit 3 = Channel 4 out of range bit 2 = Channel 3 out of range bit 1 = Channel 2 out of range bit 0 = Channel 1 out of range
In-1	Channel 1 input value
In-2	Channel 2 input value
In-3	Channel 3 input value
In-4	Channel 4 input value
Out-0 (Resolution)	Bitmap (bit 0 is LSB) bits 7-15 not used bit 6 = Display Overrange in Status bit 5 = Offset and extended range enabled bit 4 = set for Unipolar, clear for Bipolar bit 3 = Channel 4 Expanded Range (set for 0-10V range, clear for 0-1V range) bit 2 = Channel 3 Expanded Range bit 1 = Channel 2 Expanded Range bit 0 = Channel 1 Expanded Range

Table 6.5: ADU 206 output register map

4x Register	Description
Out-0 (Resolution)	Bitmap (bit 0 is LSB) bits 7-15 not used bit 6 = Display Overrange in Status bit 5 = Offset and extended range enabled bit 4 = set for Unipolar, clear for Bipolar bit 3 = Channel 4 Expanded Range (set for 0-10V range, clear for 0-1V range) bit 2 = Channel 3 Expanded Range bit 1 = Channel 2 Expanded Range bit 0 = Channel 1 Expanded Range
Out-1 (Resolution)	bits 9-15 not used bit 8 = clear for Unsigned, set for Signed bits 0-7 = decimal value to set the number of bits of resolution (11-16)

ADU 210 (4-point Voltage/Current Analog Input)

Modicon Module ID: x38 (56), NRD Module ID: x31 (49)

The ADU 210 uses four 4x-register inputs (In-0 through In-3) and two 4x-register outputs (Out-0 and Out-1). The input registers show the analog values for Channels 1 through 4 while the output registers set the Channel configuration.

NOTE: The ADU 210 must have external 24Vdc power to function properly. The ADU 210 reports an incorrect module ID (255 instead of 56) when missing the external 24Vdc. The CERI will indicate that the slot in question contains the TST 999 card instead of the ADU 210 while the ADU 210 is not powered.

Table 6.6: ADU 210 input register map

4x Register	Description
In-0	Channel 1 input value
In-1	Channel 2 input value
In-2	Channel 3 input value
In-3	Channel 4 input value

NOTE: The values used in the two output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.7: ADU 210 output register map

4x Register	Description
Out-0 (Channels 1 and 2 configuration)	High byte = Channel 1 configuration (hex values) 01 = 0 to 10V 09 = 2 to 10V 02 = 0 to 5V (0 to 20mA) 0A = 1 to 5V (4 to 20mA) 11 = 0 to 10V – Limit <> 0 19 = 0 to 10V – Limit <> 0 12 = 0 to 5V (0 to 20mA) – Limit <> 0 1A = 1 to 5V (4 to 20mA) – Limit <> 0 21 = +/-10V 22 = +/-5V (+/-20mA) Low byte = Channel 2 configuration
Out-1 (Channels 3 and 4 configuration)	High byte = Channel 3 configuration Low byte = Channel 4 configuration

ADU 211 (8-point Universal Isolated Analog Input)

Modicon Module ID: x76 (118), NRD Module ID: x23 (35)

The ADU 211 uses eighteen 4x-register inputs (In-0 through In-17) and three 4x-register outputs (Out-0 through Out-2). The input registers show the analog values for Channels 1 through 4 while the output registers set the Channel configuration.

NOTE: The values used in the three output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.8: ADU 211 input register map

4x Register	Description
In-0	Channel 1 input value (low word)
In-1	Channel 1 input value (high word)
In-2	Channel 2 input value (low word)
In-3	Channel 2 input value (high word)
In-4	Channel 3 input value (low word)
In-5	Channel 3 input value (high word)
In-6	Channel 4 input value (low word)
In-7	Channel 4 input value (high word)
In-8	Channel 5 input value (low word)
In-9	Channel 5 input value (high word)
In-10	Channel 6 input value (low word)
In-11	Channel 6 input value (high word)
In-12	Channel 7 input value (low word)
In-13	Channel 7 input value (high word)
In-14	Channel 8 input value (low word)
In-15	Channel 8 input value (high word)
In-16	Bits 8-15, Range Error (bit 15 = channel 1) Bits 0-7, Data Valid (bit 0=channel 8)
In-17	Bit 2 = Module Memory Fault bit 3 = Module Hardware Fault (bit 0 is LSB)

Table 6.9: ADU 211 output register map

4x Register	Description
Out-0	Refer to Modicon I/O User Guide
Out-1	Refer to Modicon I/O User Guide
Out-2	Reserved for Modicon future use

ADU 212 (8-point Universal Isolated Analog Input)

Modicon Module ID: x76 (118), NRD Module ID: x24 (36)

The ADU 212 uses eighteen 4x-register inputs (In-0 through In-17) and three 4x-register outputs (Out-0 through Out-2). The input registers show the analog values for Channels 1 through 4 while the output registers set the Channel configuration.

> **NOTE**: The values used in the three output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.10: ADU 212 input register map

4x Register	Description
In-0	Channel 1 input value (low word)
In-1	Channel 1 input value (high word)
In-2	Channel 2 input value (low word)
In-3	Channel 2 input value (high word)
In-4	Channel 3 input value (low word)
In-5	Channel 3 input value (high word)
In-6	Channel 4 input value (low word)
In-7	Channel 4 input value (high word)
In-8	Channel 5 input value (low word)
In-9	Channel 5 input value (high word)
In-10	Channel 6 input value (low word)
In-11	Channel 6 input value (high word)
In-12	Channel 7 input value (low word)
In-13	Channel 7 input value (high word)
In-14	Channel 8 input value (low word)
In-15	Channel 8 input value (high word)
In-16	Bits 8-15, Range Error (bit 15 = channel 1) Bits 0-7, Data Valid (bit 0=channel 8)
In-17	Bit 2 = Module Memory Fault bit 3 = Module Hardware Fault (bit 0 is LSB)

Table 6.11: ADU 212 output register map

4x Register	Description
Out-0	Refer to Modicon I/O User Guide
Out-1	Refer to Modicon I/O User Guide
Out-2	Reserved for Modicon future use

ADU 214 (8-point Non-Isolated Analog Input)

Modicon Module ID: x24 (36), NRD Module ID: x17 (23)

The ADU 212 uses eight 4x-register inputs (In-0 through In-7) and four 4x-register outputs (Out-0 through Out-3). The input registers show the analog values for Channels 1 through 8 while the output registers set the Channel configuration.

> **NOTE**: The values used in the four output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.12: ADU 214 input register map

4x Register	Description
In-0	Channel 1 input value
In-1	Channel 2 input value
In-2	Channel 3 input value
In-3	Channel 4 input value
In-4	Channel 5 input value
In-5	Channel 6 input value
In-6	Channel 7 input value
In-7	Channel 8 input value

Table 6.13: ADU 214 output register map

4x Register	Description
Out-0	Refer to Modicon I/O User Guide
Out-1	Refer to Modicon I/O User Guide
Out-2	Refer to Modicon I/O User Guide
Out-3	Refer to Modicon I/O User Guide

ADU 216 (8-point Thermocouple Isolated Analog Input)

Modicon Module ID: x3B (59), NRD Module ID: x1D (29)

The ADU 216 uses nine 4x-register inputs (In-0 through In-3) and one 4x-register output (Out-0). The input registers show the status and analog values for Channels 1 through 8 while the output register sets the Channel configuration.

> **NOTE**: The values used in the output register are typically set through the Configuration page on the CERI's Web server. These values will not

change during normal operation and do not need to be written by the controlling PLC. It is advised that this output register not be included in the I/O Scanner writes.

Table 6.14: ADU 216 input register map

4x Register	Description
In-0 (Status)	bits 8-15 are not used. bit 7 = module ready if set, not ready/defect if clear bit 6 = reference sensor open circuit if set bit 5 = open circuit or over-temperature if set bits 4-2 = channel number with open circuit detected (binary value) bit 1 = channel 8 input, 0=terminals 20&21, 1=reference sensor bit 0 = not used
In-1	Channel 1 input value
In-2	Channel 2 input value
In-3	Channel 3 input value
In-4	Channel 4 input value
In-5	Channel 5 input value
In-6	Channel 6 input value
In-7	Channel 7 input value
In-8	Channel 8 input value (or reference sensor)

Table 6.15: ADU 216 output register map

4x Register	Description
Out-0 (Configuration)	Bits 5-15 are not used bits 2-4 thermocouple type 000=K, 010=J, 111=linear voltage bits 1 channel 8 input, 0=terminals 20&21, 1=reference sensor bit 0 not used

ADU 254 (4-point Voltage/RTD Analog Input)

Modicon Module ID: x20 (32), NRD Module ID: x3A (58)

The ADU 254 uses four 4x-registers (In-0 through In-3) for the analog data from Channels 1 through 4. There are no output registers assigned to this card.

Table 6.16: ADU 254 input register map

4x Register	Description
In-0	Channel 1 input value
In-1	Channel 2 input value
In-2	Channel 3 input value
In-3	Channel 4 input value

ADU 256 (4-point Voltage/Current Isolated Analog Input)

Modicon Module ID: x2A (42), NRD Module ID: x23 (35)

The ADU 256 use five 4x-register inputs (In-0 through In-4) and two 4x-register outputs (Out-0 and Out-1). The input registers show the status and analog values for Channels 1 through 4 while the output registers set the resolution and Channel configuration.

> **NOTE**: The values used in the two output registers are typically set through the Configuration page on the CERI's Web server. These values will not change during normal operation and do not need to be written by the controlling PLC. It is advised that these outputs not be included in the I/O Scanner writes.

Table 6.17: ADU 256 input register map

4x Register	Description
In-0 (Status)	Bitmap (bit 0 is LSB) bits 8-15 not used bit 7 = set on Fault bit 6 = set if external supply bad bit 5 = Offset and extended resolution turned on bit 4 = set if Unipolar, clear if Bipolar bit 3 = Channel 4 out of range bit 2 = Channel 3 out of range bit 1 = Channel 2 out of range bit 0 = Channel 1 out of range
In-1	Channel 1 input value
In-2	Channel 2 input value
In-3	Channel 3 input value
In-4	Channel 4 input value
Out-0 (Resolution)	Bitmap (bit 0 is LSB) bits 7-15 not used bit 6 = Display Overrange in Status bit 5 = Offset and extended range enabled bit 4 = set for Unipolar, clear for Bipolar bit 3 = Channel 4 Expanded Range (set for 0-10V range, clear for 0-1V range) bit 2 = Channel 3 Expanded Range bit 1 = Channel 2 Expanded Range bit 0 = Channel 1 Expanded Range

Table 6.18: ADU 256 output register map

4x Register	Description
Out-0 (Resolution)	Bitmap (bit 0 is LSB) bits 7-15 not used bit 6 = Display Overrange in Status bit 5 = Offset and extended range enabled bit 4 = set for Unipolar, clear for Bipolar bit 3 = Channel 4 Expanded Range (set for 0-10V range, clear for 0-1V range) bit 2 = Channel 3 Expanded Range bit 1 = Channel 2 Expanded Range bit 0 = Channel 1 Expanded Range
Out-1 (Resolution)	bits 9-15 not used bit 8 = clear for Unsigned, set for Signed bits 0-7 = decimal value to set the number of bits of resolution (11-16)

ADU 257 (8-point mV/RTD/TC/Resistance Analog Input)

The ADU 257 requires the same 20 input register layout as with the Compact PLC.

Table 6.19: ADU 257 input register map

4x Register	Description
In-0	Input Status Word.
In-1	Input Status Word
In-2	Input #1 data (low word)
In-3	Input #1 data (high word)
In-4	Input #2 data (low word)
In-5	Input #2 data (high word)
In-6	Input #3 data (low word)
In-7	Input #3 data (high word)
In-8	Input #4 data (low word)
In-9	Input #4 data (high word)
In-10	Input #5 data (low word)
In-11	Input #5 data (high word)
In-12	Input #6 data (low word)
In-13	Input #6 data (high word)
In-14	Input #7 data (low word)
In-15	Input #7 data (high word)
In-16	Input #8 data (low word)
In-17	Input #8 data (high word)
In-18	Input #9 data (cold junction sensor) (low word)
In-19	Input #9 data (cold junction sensor) (high word)

Table 6.20: ADU 257 output register map

4x Register	Description
Out-0	MSB = Temperature & CJC Settings LSB = Ch. 1 Config
Out-1	MSB = Ch 2 Config LSB = Ch 3 Config
Out-2	MSB = Ch 4 Config LSB = Ch 5 Config
Out-3	MSB = Ch 6 Config LSB = Ch 7 Config
Out-4	MSB = Ch 8 Config LSB = Reserved = 0

BKF 201 (Interbus S Master)

16 Word Modicon Module ID: x5C (92), NRD Module ID: x37 (55)

64 Word Modicon Module ID: x5D (93), NRD Module ID: x38 (56)

The BKF 201 may be configured for either 16 output/input registers or 64 output/input registers. The register layout and operation is the same for the CERI as with the Compact PLC.

DIP Switch S0=ON and S1=OFF sets the BKF 201 for 16 word operation.

DIP Switch S0=ON and S1=ON sets the BKF 201 for 64 word operation.

NOTE: 64 register operation is valid only in the primary CPU rack. Sixteen register operation is valid in the primary and all expansion racks.

Table 6.21: BFK 201 input register map

4x Register	Description
In-0 (Status)	Bits 15-8 display the configuration checksum Bits 7-5 not used. Bits 4-0 Status bitmap.
In-1	Interbus data – Input word 1
In-2	Interbus data – Input word 2
...	...
In-15 or In-63	Interbus data – Input word 15 or Input word 63

Table 6.22: BFK 201 output register map

4x Register	Description
Out-0	Bits 15-8 bus configuration checksum (copy from In-0 high byte) Bits 7-0 command value bit 1 = alarm stop bit 2 = start cycle bit 3 = quit error bit 4 = not used bits 3 and 5 only = get configuration
Out-1	Interbus data – Output word 1
Out-2	Interbus data – Output word 2
...	...
Out-15 or Out-63	Interbus data – Output word 15 or Output word 63

DAO 216 (16-point 24Vdc Non-isolated Discrete Output)

Modicon Module ID: x1B (27), NRD Module ID: x11 (17)

The DAO 216 only uses one (Out-0) 4x-register for its 16 discrete outputs.

Table 6.23: DAO 216 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DAP 204 (4-point Relay Discrete Output)

Modicon Module ID: x17 (23), NRD Module ID: x0D (13)

The DAP 204 only uses one 4x-register (Out-0) for its 4 discrete Outputs. Bits 4-15 are not used.

Table 6.24: DAP 204 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAP 208 (8-point Relay Discrete Output)

Modicon Module ID: x0F (15), NRD Module ID: x07 (07)

The DAP 208 only uses one 4x-register (Out-0) for its 8 discrete Outputs. Bits 8-15 are not used.

Table 6.25: DAP 208 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)									1	2	3	4	5	6	7	8

DAP 210 (8-point 24..240 Vac Discrete Output)

Modicon Module ID: x10 (16), NRD Module ID: x08 (08)

The DAP 210 only uses one 4x-register (Out-0) for its 8 discrete Outputs. Bits 8-15 are not used.

Table 6.26: DAP 210 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)									1	2	3	4	5	6	7	8

DAP 211 (Monitored 4-point Out Combined I/O)

Modicon Module ID: x0A (10), NRD Module ID: x03 (03)

The DAP 211 uses one 4x-register (In-0) for its 4 discrete Inputs and one 4x-register (Out-0) for its 4 discrete Outputs. Bits 4-15 are not used on In-0 and bits 4-15 are not used on Out-0.

Table 6.27: DAP 211 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)													1	2	3	4

Table 6.28: DAP 211 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAP 212 (8-point In/4-point Out Combined I/O)

Modicon Module ID: x08 (08), NRD Module ID: x01 (01)

The DAP 212 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 4 discrete Outputs. Bits 8-15 are not used on In-0 and bits 4-15 are not used on Out-0.

Table 6.29: DAP 212 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.30: DAP 212 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAP 216 (16-point 24Vdc Discrete Output)

Modicon Module ID: x19 (25), NRD Module ID: x0F (15)

The DAP 216 only uses one (Out-0) 4x-register for its 16 discrete outputs.

Table 6.31: DAP 216 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DAP 217 (16-point 5-24Vdc Discrete Output True Low)

Modicon Module ID: x2A (42), NRD Module ID: x18 (24)

The DAP 217 only uses one (Out-0) 4x-register for its 16 discrete outputs.

Table 6.32: DAP 217 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DAP 218 (16-point 24-249Vac Discrete Output)

Modicon Module ID: x1D (29), NRD Module ID: x13 (19)

The DAP 218 only uses one (Out-0) 4x-register for its 16 discrete outputs.

Table 6.33: DAP 218 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DAP 220 (8-point In/8-point Out Combined I/O)

Modicon Module ID: x09 (9), NRD Module ID: x02 (2)

The DAP 220 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 8 discrete Outputs. Bits 8-15 are not used on In-0 and bits 8-15 are not used on Out-0.

Table 6.34: DAP 220 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.35: DAP 220 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)									1	2	3	4	5	6	7	8

DAP 250 (8-point In/8-point Out Combined I/O)

Modicon Module ID: x09 (9), NRD Module ID: x39 (57)

The DAP 250 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 8 discrete Outputs. Bits 8-15 are not used on In-0 and bits 8-15 are not used on Out-0.

Table 6.36: DAP 250 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.37: DAP 250 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)									1	2	3	4	5	6	7	8

DAP 252 (8-point In/4-point Out Combined I/O)

Modicon Module ID: x08 (8), NRD Module ID: x32 (50)

The DAP 252 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 4 discrete Outputs. Bits 8-15 are not used on In-0 and bits 4-15 are not used on Out-0.

Table 6.38: DAP 252 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.39: DAP 252 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAP 253 (8-point In/4-point Out Combined I/O)

Modicon Module ID: x08 (8), NRD Module ID: x33 (51)

The DAP 253 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 4 discrete Outputs. Bits 8-15 are not used on In-0 and bits 4-15 are not used on Out-0.

Table 6.40: DAP 253 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.41: DAP 253 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAP 258 (8-point Relay Discrete Output)

Modicon Module ID: x18 (24), NRD Module ID: x2B (43)

The DAP 258 only uses one 4x-register (Out-0) for its 8 discrete Outputs. Bits 8-15 are not used.

Table 6.42: DAP 258 register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)									1	2	3	4	5	6	7	8

DAP 292 (8-point In/4-point Out Combined I/O)

Modicon Module ID: x08 (8), NRD Module ID: x34 (52)

The DAP 292 uses one 4x-register (In-0) for its 8 discrete Inputs and one 4x-register (Out-0) for its 4 discrete Outputs. Bits 8-15 are not used on In-0 and bits 4-15 are not used on Out-0.

Table 6.43: DAP 292 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

Table 6.44: DAP 292 output register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Out-0 (Output #)													1	2	3	4

DAU 202 (2-point Voltage/Current Analog Output)

Modicon Module ID: x30 (48), NRD Module ID: x1B (27)

The DAU 202 uses three 4x-registers (Out-0 through Out-2). The first register configures the resolution while the second and third set output values for Channels 1 and 2.

Table 6.45: DAU 202 output register map

4x Register	Description
Out-0 (LSB Resolution MSB Hold Last Value)	LSB Value 0 = 15 bit + sign LSB Value 6 = 12 bit bit 8 = Channel 1 Hold Last Value (1=Hold, 0=User Default bit 9 = Channel 2 Hold Last Value (1=Hold, 0=User Default
Out-1	Channel 1 output value (-32768 to 32752 or 0 to 4095)
Out-2	Channel 2 output value (-32768 to 32752 or 0 to 4095)

Each output channel of the DAU 202 may be independently configured to Hold Last Value or revert to a User Default value when the CERI is halted.

Table 6.46: DAU 202 Output Operating Values

Voltage (Vdc)	Current (mA)	12-bits	15-bits + sign	Range
<-10	<-20	0..47	-32768...-32016	Under
-10	-20	48	-32000	Normal
0	0	2048	0	
10	20	4048	32000	
>10	>20	4049..4095	+32016...+32752	Over

DAU 204 (4-point Voltage/Current Analog Output)

Modicon Module ID: x75 (117), NRD Module ID: x22 (34)

> **NOTE**: The DAU 204 must be powered when in the rack and the power switch on the CERI must not be turned off while the DAU 204 is powered. The 24Vdc power used for the CERI should also be the same power for the DAU 204.
>
> Cycling power independently on either the CERI or DAU 204 may cause unpredictable output operation on the DAU 204.

The DAU 204 includes one 4x-register input (In-0) for status and seven registers four output and configuration (Out-0 through Out-6).

Table 6.47: DAU 204 input register bit-map

4x Register Bit #	15 (MSB)	14	13..5	4	3	2	1	0 (LSB)
In-0 (Status)	Module Error	Module Memory Error	Not USed	Ch 4 Current Error	Ch 3 Current Error	Ch 2 Current Error	Ch 1 Current Error	Current Error

Table 6.48: DAU 204 output register map

4x Register	Description
Out-0 (LSB Resolution MSB Hold Last Value)	LSB Value 0 = 15 bit + sign LSB Value 6 = 12 bit bit 8 = Channel 1 Hold Last Value (1=Hold, 0=User Default bit 9 = Channel 2 Hold Last Value (1=Hold, 0=User Default
Out-0	Channel 1 output value (-32768 to 32752 or 0 to 4095)
Out-1	Channel 2 output value (-32768 to 32752 or 0 to 4095)
Out-2	Channel 3 output value (-32768 to 32752 or 0 to 4095)
Out-3	Channel 4 output value (-32768 to 32752 or 0 to 4095)
Out-4	Control Word 0, Range Select
Out-5	Control Word 1, Fault State
Out-6	Control Word 2, Scaling

The Range Select includes a nybble for each output channel. The least significant nybble selects channel 0 while the most significant nybble selects channel 4.

Table 6.49: DAU 204 Range Values

Nybble value	Range
0	4..20mA
1	0..20mA
2	0..1V
3	+/-1V
4	0..5V
5	+/-5V
6	0..10V
7	-10...+10V

The Fault State word include configuration for hold last value (bits8-11) and

other calibration and test mode bits. Refer to the IO User guide for information on calibrating the DAU 204.

Table 6.50: DAU 204 Fault State register bit-map

4x Register Bit #	15 (MSB)	14-12	11	10	9	8	7-0 (LSB)
Out-5 (Fault State)	Calibration	Test Mode	Ch 4 Hold Last Value	Ch 3 Hold Last Value	Ch 2 Hold Last Value	Ch 1 Hold Last Value	Calibration

Each output channel of the DAU 204 may be independently configured to Hold Last Value or revert to a User Default value when the CERI is halted.

The Scale Select includes a nybble for each output channel. The least significant nybble selects channel 0 while the most significant nybble selects channel 4.

NOTE: The loadable used in Concept for 15-bit+sign functions as expected on +/- voltage ranges with -32000,0,+32000 values corresponding with -full scale, zero, and +full scale. The loadable used in ProWORX32 and ProWORXnXT for 15-bit+sign actually functioned as a 14-bit setting. See Table 6.54

Table 6.51: DAU 204 Scale Values

Nybble value	Scale
0	12-bit
1	11-bit
2	15-bit + Sign (Concept)
3	16-bit
4	15-bit + Sign (ProWORX)

Table 6.52: DAU 204 Output Operating Values for 0-1, 0-5, 0-10 VDC

0...1 Vdc	0...5 Vdc	0..10 Vdc	11-bits	12-bits	15-bits + sign (ProWORX)	15-bits + sign (Concept)	16-bits
0	0	0	0	0	0	0	0
0.5	2.5	5	1024	2048	16000	16000	32768
1	5	10	2047	4095	32000	32000	65520

Table 6.53: DAU 204 Output Operating Values for 0/4...20mA

0...20 mA	4...20 mA	11-bits	12-bits	15-bits + sign (ProWORX)	15-bits + sign (Concept)	16-bits
0	4	0	0	0	0	0
10	12	1024	2048	16000	16000	32768
20	20	2047	4095	32000	32000	65520

Table 6.54: DAU 204 Output Operating Values for +/-1, +/-5, +/-10 VDC

+/-1 Vdc	+/-5 Vdc	+/-10 Vdc	11-bits	12-bits	15-bits + sign (ProWORX)	15-bits + sign (Concept)	16-bits
-1	-5	-10	0	0	0	-32000	0
0	0	0	1024	2048	16000	0	32768
1	5	10	2047	4095	32000	32000	65520

DAU 208 (8-point +/-10Vdc Isolated Analog Output)

Modicon Module ID: x32 (50) , NRD Module ID: x1C (28)

The DAU 208 uses nine 4x-registers (Out-0 through Out-8). The first register configures the resolution and hold last value while the rest set output values for Channels 1 through 8.

Table 6.55: DAU 208 output register map

4x Register	Description
Out-0 (LSB Resolution MSB Hold Last Value)	LSB Value 0 = 15 bit + sign LSB Value 6 = 12 bit bit 8 = Channel 1 Hold Last Value (1=Hold, 0=User Default bit 9 = Channel 2 Hold Last Value (1=Hold, 0=User Default bit 10 = Channel 3 Hold Last Value (1=Hold, 0=User Default bit 11 = Channel 4 Hold Last Value (1=Hold, 0=User Default bit 12 = Channel 5 Hold Last Value (1=Hold, 0=User Default bit 13 = Channel 6 Hold Last Value (1=Hold, 0=User Default bit 14 = Channel 7 Hold Last Value (1=Hold, 0=User Default bit 15 = Channel 8 Hold Last Value (1=Hold, 0=User Default
Out-1	Channel 1 output value (-32768 to 32752 or 0 to 4095)
Out-2	Channel 2 output value (-32768 to 32752 or 0 to 4095)
Out-3	Channel 3 output value (-32768 to 32752 or 0 to 4095)
Out-4	Channel 4 output value (-32768 to 32752 or 0 to 4095)
Out-5	Channel 5 output value (-32768 to 32752 or 0 to 4095)
Out-6	Channel 6 output value (-32768 to 32752 or 0 to 4095)
Out-7	Channel 7 output value (-32768 to 32752 or 0 to 4095)
Out-8	Channel 8 output value (-32768 to 32752 or 0 to 4095)

Each output channel of the DAU 208 may be independently configured to Hold Last Value or revert to a User Default value when the CERI is halted.

Table 6.56: DAU 208 Output Operating Values

Voltage (Vdc)	12-bits	15-bits + sign	Range
<-10	0..47	-32768...-32016	Under
-10	48	-32000	Normal
0	2048	0	
10	4048	32000	
>10	4049..4095	+32016...+32752	Over

DAU 252 (2-point Voltage/Current Analog Output)

Modicon Module ID: x30 (48), NRD Module ID: x3B (59)

The DAU 252 uses three 4x-registers (Out-0 through Out-2). The first register configures the resolution while the second and third set output values for Channels 1 and 2.

Table 6.57: DAU 252 output register map

4x Register	Description
Out-0 (LSB Resolution MSB Hold Last Value)	LSB Value 0 = 15 bit + sign LSB Value 6 = 12 bit bit 8 = Channel 1 Hold Last Value (1=Hold, 0=User Default bit 9 = Channel 2 Hold Last Value (1=Hold, 0=User Default
Out-1	Channel 1 output value (-32768 to 32752 or 0 to 4095)
Out-2	Channel 2 output value (-32768 to 32752 or 0 to 4095)

Each output channel of the DAU 202 may be independently configured to Hold Last Value or revert to a User Default value when the CERI is halted.

Table 6.58: DAU 252 Output Operating Values

Voltage (Vdc)	Current (mA)	12-bits	15-bits + sign	Range
<-10	<-20	0..47	-32768...-32016	Under
-10	-20	48	-32000	Normal
0	0	2048	0	
10	20	4048	32000	
>10	>20	4049..4095	+32016...+32752	Over

DEO 216 (16-point 24Vdc Non-Isolated Discrete Input)

Modicon Module ID: x0D (13), NRD Module ID: x05 (5)

The DEO 216 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.59: DEO 216 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 208 (8-point 230Vac Discrete Input)

Modicon Module ID: x0F (15), NRD Module ID: x07 (7)

The DEP 208 only uses one 4x-register (In-0) for its 8 discrete inputs. Bits 8-15 are not used.

Table 6.60: DEP 208 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

DEP 209 (8-point 120Vac Discrete Input)

Modicon Module ID: x13 (19), NRD Module ID: x0B (11)

The DEP 209 only uses one 4x-register (In-0) for its 8 discrete inputs. Bits 8-15 are not used.

Table 6.61: DEP 209 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

DEP 210 (8-point 115 Vac Discrete Input)

Modicon Module ID: x10 (16), NRD Module ID: x08 (8)

The DEP 210 only uses one 4x-register (In-0) for its 8 discrete inputs. Bits 8-15 are not used.

Table 6.62: DEP 210 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

DEP 211 (8-point 115 Vac Isolated Discrete Input)

Modicon Module ID: x11 (17), NRD Module ID: x09 (9)

The DEP 211 only uses one 4x-register (In-0) for its 8 discrete inputs. Bits 8-15 are not used.

Table 6.63: DEP 211 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)									1	2	3	4	5	6	7	8

DEP 214 (16-point 10-60Vdc Discrete Input)

Modicon Module ID: x14 (20), NRD Module ID: x0C (12)

The DEP 214 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.64: DEP 214 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 215 (16-point 5Vdc TTL True Low Discrete Input)

Modicon Module ID: x2E (46), NRD Module ID: x1A (26)

The DEP 215 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.65: DEP 215 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 216 (16-point 24Vdc Discrete Input)

Modicon Module ID: x0C (12), NRD Module ID: x04 (4)

The DEP 216 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.66: DEP 216 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 217 (16-point 24Vdc Discrete Input)

Modicon Module ID: x2D (45), NRD Module ID: x19 (25)

The DEP 217 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.67: DEP 217 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 218 (16-point 115VAC Discrete Input)

Modicon Module ID: x12 (18), NRD Module ID: x0A (10)

The DEP 218 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.68: DEP 218 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 254 (16-point 10-60Vdc Discrete Input)

Modicon Module ID: x14 (20), NRD Module ID: x3C (60)

The DEP 254 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.69: DEP 254 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 256 (16-point 24Vdc Discrete Input Extended Temp.)

Modicon Module ID: x0C (12), NRD Module ID: x2C (44)

The DEP 256 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.70: DEP 256 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 257 (16-point 110Vdc Discrete Input)

Modicon Module ID: x0C (12), NRD Module ID: x2D (45)

The DEP 257 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.71: DEP 257 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 296 (16-point 60Vdc Isolated Discrete Input)

Modicon Module ID: x0C (12), NRD Module ID: x2E (46)

The DEP 296 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.72: DEP 296 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DEP 297 (16-point 48Vdc Isolated Discrete Input)

Modicon Module ID: x0C (12), NRD Module ID: x2F (47)

The DEP 297 only uses one 4x-register (In-0) for its 16 discrete inputs.

Table 6.73: DEP 297 input register bit-map

4x Register Bit #	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
In-0 (Input #)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

MOT 201 (Motion Module)

Modicon Module ID: x6E (110), NRD Module ID: x20 (32)

The CERI uses the same 6 register in/out layout of the Compact PLC.

Table 6.74: MOT 201 input register map

4x Register	Description
In-0	Status
In-1	Echo of command register
In-2	Data register 1
In-3	Data register 2
In-4	Data register 3
In-5	Data register 4

Table 6.75: MOT 201 output register map

4x Register	Description
Out-0	Control register
Out-1	Command register
Out-2	Data register 1
Out-3	Data register 2
Out-4	Data register 3
Out-5	Data register 4

MOT 202 (Motion Module)

Modicon Module ID: x6F (111), NRD Module ID: x21 (33)

The CERI uses the same 6 register in/out layout of the Compact PLC.

Table 6.76: MOT 202 input register map

4x Register	Description
In-0	Status
In-1	Echo of command register
In-2	Data register 1
In-3	Data register 2
In-4	Data register 3
In-5	Data register 4

Table 6.77: MOT 202 output register map

4x Register	Description
Out-0	Control register
Out-1	Command register
Out-2	Data register 1
Out-3	Data register 2
Out-4	Data register 3
Out-5	Data register 4

TST 999 (NR&D Test Module)

Modicon Module ID: x7F (127), NRD Module ID: x35 (53)

The TST 999 module uses 32 registers of input (IN-0 through IN-31) and 32 registers of output (OUT-0 through OUT-31).

UCM 001 (NR&D Communications Module)

Modicon Module ID: x40 (64), NRD Module ID: x36 (54)

The CUCM uses 32 registers of input (IN-0 through IN-31) and 32 registers of output (OUT-0 through OUT-31). The actual meaning of each register is dependent upon the user program loaded into the CUCM.

ZAE 201 (Counter/Position Module)

Modicon Module ID: x60 (96), NRD Module ID: x1E (30)

Table 6.78: ZAE 201 input register map

4x Register	Description
In-0	Status
In-1	Position or Count (high word)
In-2	Position or Count (low word)

Table 6.79: ZAE 201 register map

4x Register	Description
Out-0	Command Word
Out-1	Target Position (high word)
Out-2	Target Position (low word)
Out-3	Parameter 1
Out-4	Parameter 2 (P1 high word)
Out-5	Parameter 3 (P1 low word)
Out-6	Parameter 4 (P2 high word)
Out-7	Parameter 5 (P2 low word)
Out-8	Parameter 6 (P3 high word)
Out-9	Parameter 7 (P3 low word)

ZAE 204 (High Speed Counter)

Modicon Module ID: x61 (97), NRD Module ID: x1F (31)

Table 6.80: ZAE 204 input register map

4x Register	Description
In-0 (Status) (Bit-Map)	bit 15 (msb) = Comms Loss bit 14 = Module Unhealthy (wrong personality code read) bits 13,12 = Unused bit 11 = Channel 4 has exceeded the target count bit 10 = Channel 3 has exceeded the target count bit 9 = Channel 2 has exceeded the target count bit 8 = Channel 1 has exceeded the target count bit 7 = Channel 4 has reached the target count bit 6 = Channel 3 has reached the target count bit 5 = Channel 2 has reached the target count bit 4 = Channel 1 has reached the target count bit 3 = Channel 4 count gate input is 12-30V bit 2 = Channel 3 count gate input is 12-30V bit 1 = Channel 2 count gate input is 12-30V bit 0 (lsb) = Channel 1 count gate input is 12-30V
In-1 (Channel 4) (Error Code) (Decimal Value)	0 = No Error 1 = Differential and 10kHz requested on channel 1 2 = Differential and repetitive mode requested on channels 1 or 3 3 = 10kHz operation requested on channels 2, 3, or 4 4 = Mode change requested on channels 2 or 4 while channels 1 or 3 are set for differential operation 5 = Differential operation requested on channels 2 or 4 6 = Invalid target value has been specified
In-2	Channel 3 Error Code
In-3	Channel 2 Error Code
In-4	Channel 1 Error Code
In-5	Channel 4 Current Count
In-6	Channel 3 Current Count
In-7	Channel 2 Current Count
In-8	Channel 1 Current Count

Table 6.81: ZAE 204 register map

4x Register	Description
Out-0 (Counter 1) (Mode Bit-Map)	bits 15-7 = unused bit 6 = Count direction (1=up) bit 5 = Active level for counter output channel (1=Active Low) bit 4 = Count enable config (1=High enable allows counting) bit 3 = Transition level for count (1=Negative edge) bit 2 = 10kHz operation (channel 1 only) (1=10kHz) bit 1 = Differential mode operation (channels 1 & 3 only) (1=Diff)
Out-1	Counter 1 Target Count
Out-2	Counter 2 Mode Bit-map
Out-3	Counter 2 Target Count
Out-4	Counter 3 Mode Bit-map
Out-5	Counter 3 Target Count
Out-6	Counter 4 Mode Bit-map
Out-7	Counter 4 Target Count

7 Front Panel Operation

Keypad

The keypad includes the ⬅, ➡, ⬆, ⬇, and ↵ buttons. In general, the ⬅ button moves to the left and also acts as an "escape" key to move back one menu level. The ➡ button moves to the right and also moves down one menu level. The up and down buttons increment and decrement numbers and step up and down menu lists. The ↵ button acts as an "enter" key.

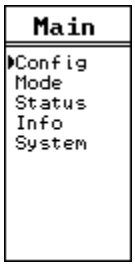
Splash Screen

The CERI splash screen shows the Nameplae (defaults to CERI when empty), IP Address (206.223.51.190), the operating mode (CONFIG, RUN, HALT), the controlling Master number (-,1,2,3,4), and error messages.

Backlight

The backlight will illuminate on any key press and will also flash on an error condition. The timeout for the backlight is configured through Modbus drop 255 register 7003 and defaults to 300 seconds.

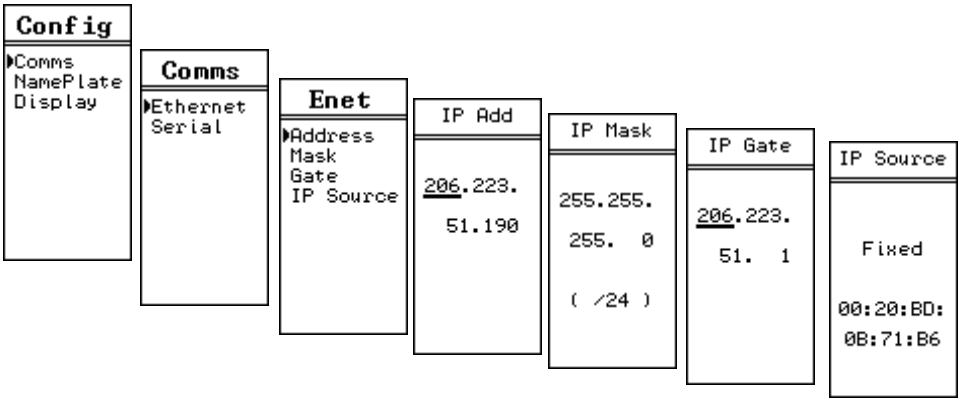
Main Screen



Pressing the ➡, ⬆, ⬇, or ↵ buttons from the splash screen will lead to the "Main" menu page. Use the ⬆ or ⬇ keys to choose the sub-menu. The ➡ or ↵ will drill down into the next menu level while the ⬅ key will back up to the splash screen.

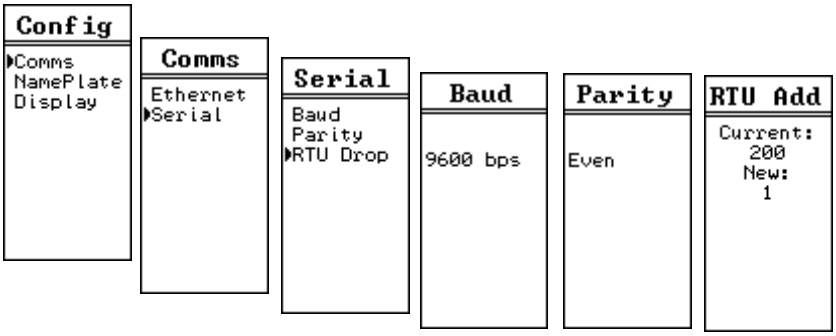
Config Screens

The Config screen allows the adjustment/viewing of the communications parameters, NamePlate, and Display settings.



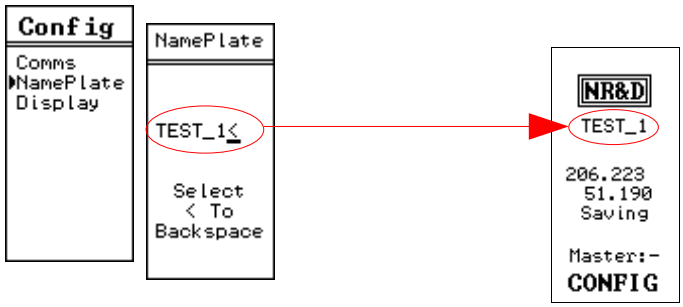
NOTE: The IP Mask automatically increments/decrements the bit mask using the UP/DOWN keys.

NOTE: The IP Source includes: Fixed, DHCP, and BOOTP.

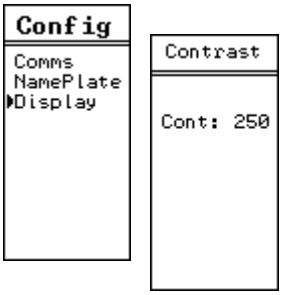


NOTE: The serial port is fixed as a Modbus RTU Slave. The baud rate and parity are adjustable. The data bits are fixed at 8 and stop bits are fixed at 1. The CERI responds to Modbus RTU messages to slaves 0, 1, or 200, 201, 202, and 255.

The RTU Address page allows the user to adjust the drop number for the virtual PLC memory from 200 to another number within the range 1-200. See Chapter 9 for more information.

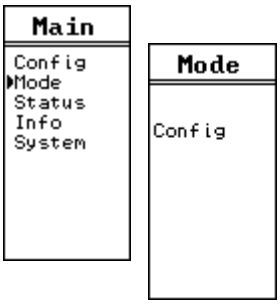


Note: Select the "<" character to backspace. Only capital letters A-Z, numbers 0-0, and underscore "_" are allowed in the nameplate. Press the ↵ key while not on a "<" character to accept the nameplate and return to the previous screen.



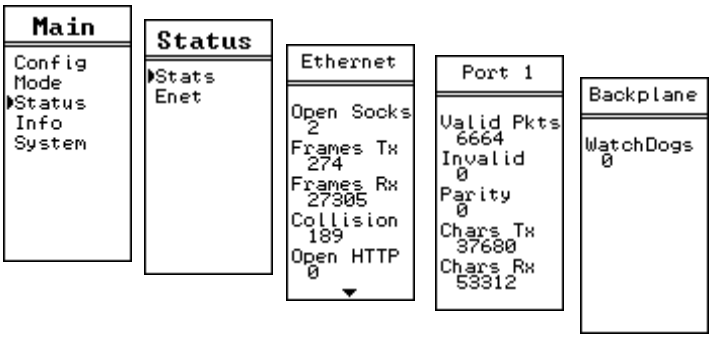
NOTE: The Contrast value may be adjusted between 240-300.

Mode Screens



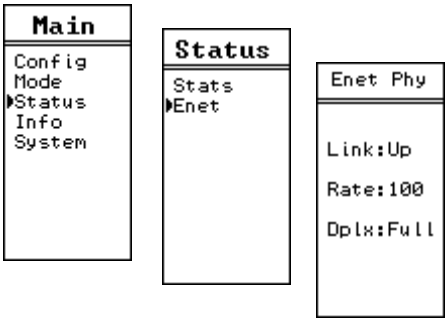
NOTE: The Mode values are Run, Config, and Halt. "Run" is a read-only configuration setting. Configuration values may be altered in "Config" or "Halt". The CERI must be in "Halt" to load new firmware. The A120 outputs are all forced to default conditions while in "Halt".

Status Screens



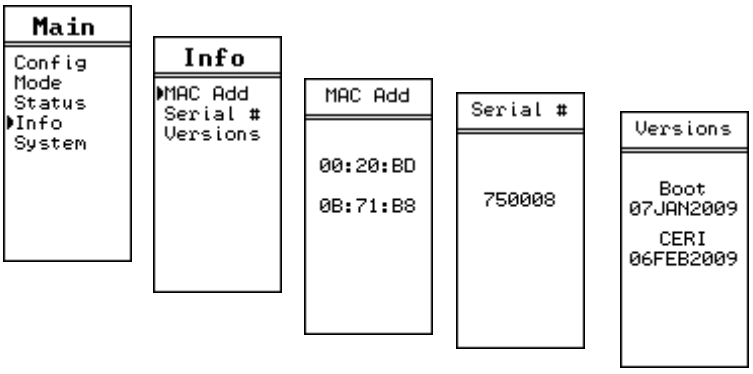
NOTE: The Stats screens may have multiple pages that are accessed using the up and down keys. Press the Enter key to return to the previous menu.

NOTE: The Backplane WatchDogs counter indicates the number of times that the controlling master has been lost and the watchdog timer has expired causing the A120 I/O to revert to the default values.

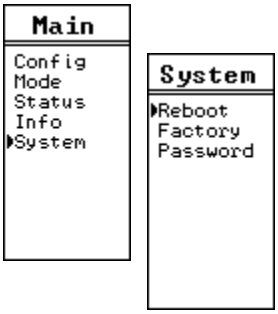


NOTE: All Stats values are zeroed on a power cycle.

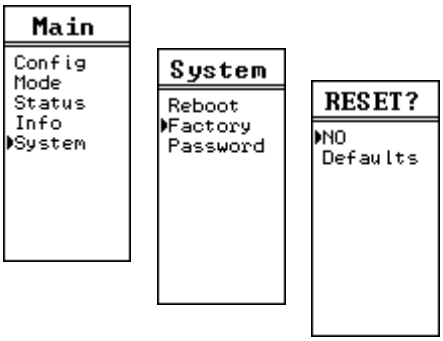
Info Screens



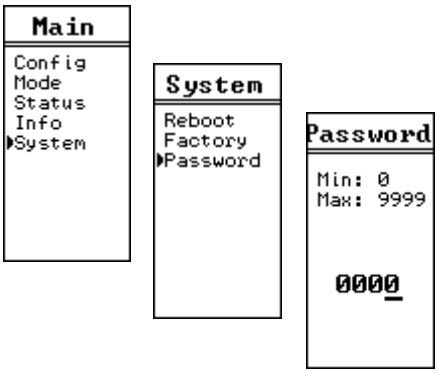
System Screen



NOTE: Pressing the ➡ or ↵ keys while “Reboot” is selected will cause an immediate reboot of the CERI. This will cause a loss of control of the A120 I/O.



NOTE: Selecting “Defaults” will result in the loss of all configuration of the CERI with a return to factory default settings.



NOTE: Selecting a password of a number greater than 0000 will cause the user to enter this password on any parameter change through the front panel. The value 0000 will disable the password feature.

NOTE: This password is not the same password used by the Web server.

8 Register List

Drop 0/1 Register List

Modbus/TCP Index 0 or 1 will access the “data” registers of the CERI. These registers are all Modbus Holding Registers (4x).

Table 8.1: Drop 0/1 Register List

Register Range	Read/ Write	Description
1-10000	Read/ Write	I/O data area
20001-30000	Read Only	Rack and slot number for registers 1-10000 (See Table 8.2)
30001-40000	Read/ Write	Default output states for registers 1-10000

Table 8.2: Rack and slot number bit assignments

Bit	Description
15 (MSB)	0 = Rack Mapper Entry 1 = Internal Mapper Entry
14-8	Internal Mapper Entry index (1-100)
14-12	Rack Mapper Entry Rack Number (1-4)
10-8	Rack Mapper Entry Slot Number (1-5)
7-6	Internal flags used by CERI, will always read zero from Modbus
5-0 (LSB)	Error condition 0=No Error

Drop 255 Register List

Modbus/TCP index 255 will access the configuration registers for the CERI. Registers 1 through 200 are the 50 possible mapper entries. Each mapper entry consists of four registers where registers 1-4 are entry 1, 5-8 are entry 2, etc. The meaning of each of the four words is dependent upon the type of entry (rack or internal). Unused Mapper entries should be zeroed.

Table 8.3: Mapper Entry Register List

Register	Mapper Entry	Entry Word Number
1	1	1
2		2
3		3
4		4
5	2	1
6		2
7		3
8		4
...	...	...
200	50	4

Table 8.4: Rack Mapper Entry Description

Entry Word	Type	Description
1	R/W	First Input Register (1-10000)
2	R/W	First Output Register (1-10000)
3	R/W	Module ID in MSB (See Table), 0 in LSB
4	R/W	NR&D's Module ID in MSB (See Table), LSB contains the Rack Number in Hi Nybble and Slot Number in Lo Nybble

Table 8.5: Internal Mapper Entry Description

Entry Word	Type	Description
1	R/W	Modbus Register A (1-10000)
2	R/W	Modbus Register B (1-65535)
3	R/W	Count (1-255)
4	R/W	Bitmap Bit 15 (msb) = 0 Bit 14 = 0 Bit 13 = Nybble/Byte Packing flag; 0=bytes, 1=nybbles Bit 12 = Unpacking flag; 1=Unpack 1 register into 2 Bit 11 = Packing flag; 1=pack 2 registers into 1 Bit 10 = Modbus Register “B” data source; 0=drop 0, 1= drop 255 Bit 9 = Revers bit order flag; 0=no reverse, 1=reverse Bit 8 = Direction flag; 0=A>B, 1=B>A Bit 7 through Bit 0 (lsb) = 0

Table 8.6: Configuration Registers

Register	Type	Description	
1001	R/W	Control Register Bitmap bit 0 (lsb) = Halt bit 3 = Memory Protect	
1002	R/W	Bitmap bit 0 = Allow RUN with a card missing (when set)	
1003-1010	R	Unused	
1011	R	Status Register Bitmap bit 0 (lsb) = Halted bit 2 = Running	
1012	R	Scan Time in 0.1mS units	
1013	R	IP Address of current master MSW	
1014	R	IP Address of current master LSW	
1015	R/W	Reconfigure Flag; self-clearing. Forces reconfigure of configurable I/O. Effective ONLY in Config Mode.	
1016-1020	R	Unused	
1021	R	Module IDs of Rack 1	Slot 3 (msb=1 is bad health)
1022	R		Slot 4 (msb=1 is bad health)
1023	R		Slot 5 (msb=1 is bad health)
1024	R	Module IDs of Rack 2	Slot 1 (msb=1 is bad health)
1025	R		Slot 2 (msb=1 is bad health)
1026	R		Slot 3 (msb=1 is bad health)
1027	R		Slot 4 (msb=1 is bad health)
1028	R		Slot 5 (msb=1 is bad health)
1029	R	Module IDs of Rack 3	Slot 1 (msb=1 is bad health)
1030	R		Slot 2 (msb=1 is bad health)
1031	R		Slot 3 (msb=1 is bad health)
1032	R		Slot 4 (msb=1 is bad health)
1033	R		Slot 5 (msb=1 is bad health)
1034	R	Module IDs of Rack 4	Slot 1 (msb=1 is bad health)
1035	R		Slot 2 (msb=1 is bad health)
1036	R		Slot 3 (msb=1 is bad health)
1037	R		Slot 4 (msb=1 is bad health)
1038	R		Slot 5 (msb=1 is bad health)

Table 8.7: Configuration Registers Cont.

Register	Type	Description
1039-1044	R	Unused
1045	R	Mapper Entry Conflict; 0=No conflict, 1=Conflict
1046	R	Register number where Mapper conflict occurs (0=no conflict)
1047	R	Wrong card in slot Error 0=All cards match mapper, 1=Wrong card in a rack **NOTE: CERI Halts on wrong card in slot error!**
1048	R	MSB = Rack Number of Wrong Card LSB = Slot Number of Wrong Card
1049	R	Card Missing Error 0=All cards match mapper, 1=Card(s) missing **NOTE: CERI will HALT if register 1002 bit 1 = 0.**
1050	R	MSB = Rack Number of Missing Card LSB = Slot Number of Missing Card
1051	R	Module Health Bad Error 0=All cards report healthy, 1=Card(s) reporting bad health.
1052	R	MSB = Rack Number of Bad Health Card LSB = Slot Number of Bad Health Card
1053	R	Configuration Checksum MSW
1054	R	Configuration Checksum LSW
1055	R	Configuration mismatches Flash (0=Match, 1=Mismatch)

Table 8.8: IP Address Settings

Register	Type	Description
2900	R/W	IP Address MSW
2901	R/W	IP Address LSW
2902	R/W	Default Gate MSW
2903	R/W	Default Gate LSW
2904	R/W	Subnet Mask MSW
2905	R/W	Subnet Mask LSW
2996	R/W	TCP port for NRDTCP (ignored)
2997	R/W	TCP Backstep
2998	R/W	TCP Downstream Timeout
2999	R/W	TCP Quiet Timeout
3000	R/W	IP Address of Allowed Master 1 (MSW)
3001	R/W	IP Address of Allowed Master 1 (LSW)
3002	R/W	IP Address of Allowed Master 2 (MSW)
3003	R/W	IP Address of Allowed Master 2 (LSW)
3004	R/W	IP Address of Allowed Master 3 (MSW)
3005	R/W	IP Address of Allowed Master 3 (LSW)
3006	R/W	IP Address of Allowed Master 4 (MSW)
3007	R/W	IP Address of Allowed Master 4 (LSW)
3008	R/W	Watchdog Timout (ms) (MSW of 32-bit Integer)
3009	R/W	Watchdog Timout (ms) (LSW of 32-bit Integer)
3011-3021	R/W	Password for HTTP access (C-style, null terminated string)
3300-3302	R	Ethernet MAC Address of this CERI
8030	R/W	Options Bitmap bit 0 (lsb); 1=Ethernet II framing, 0=SNAP (ignored) bit 2 = BOOTP enabled bit 3 = DHCP enabled

Table 8.9: Display Configuration Registers

Register	Type	Description
7000	R/W	LCD Contrast
7001	R/W	Debug Enable
7002	R/W	LCD Password
7003	R/W	Backlight Timeout (seconds)
7004	R/W	Nameplate Length (0-20)
7005-7014	R/W	Nameplate, packed ASCII
8191	R	Keyboard Latch state (for testing)

The CERI includes a block of statistics to describe the activity of each of the allowed Masters and unauthorized clients.

Table 8.10: Per Client Statistics

Unauthorized Masters	Master 1	Master 2	Master 3	Master 4	Counter Meaning
4000	4016	4032	4048	4064	TCP Connects
4001	4017	4033	4049	4065	Graceful Disconnects (FIN)
4002	4018	4034	4050	4066	TCP Closes (FIN and RST)
4003	4019	4035	4051	4067	Modbus/TCP protocol fail
4004	4020	4036	4052	4068	Modbus/TCP failed open
4005	4021	4037	4053	4069	Modbus/TCP queries
4006	4022	4038	4054	4070	Modbus/TCP replies
4007	4023	4039	4055	4071	Rejected writes
4008	4024	4040	4056	4072	Outputs control dropped
4009	4025	4041	4057	4073	Unused
4010	4026	4042	4058	4074	Unused
4011	4027	4043	4059	4075	Unused
4012	4028	4044	4060	4076	Unused
4013	4029	4045	4061	4077	Unused
4014	4030	4046	4062	4078	Unused
4015	4031	4047	4063	4079	Unused

Many of the Compact I/O share the same Module ID so the CERI uses a unique ID to define all supported cards.

Table 8.11: Module IDs

Name	Modicon ID		NR&D ID		Description	Input Words	Output Words
	Dec	Hex	Dec	Hex			
ADU204	32	20	20	14	4 Ch. RTD +/-0.5V Input	4	0
ADU205	34	22	21	15	4 Ch Analog Input	4	5
ADU206	35	23	22	16	4 Ch. Fast Analog Input	5	2
ADU210	56	38	49	31	4 Ch. Analog Input 10V	4	1
ADU211	118	76	35	23	8 Ch. V,I,Thermo Input	18	3
ADU212	118	76	36	24	8 Ch. V,I,Thermo Input	18	3
ADU214	36	24	23	17	8 Ch. V,RTD,R Input	8	4
ADU216	59	3b	29	1d	8 Ch. Thermocouple Input	9	1
ADU254	32	20	58	3a	4 Ch. RTD +/-0.5V Input	4	0
ADU256	35	23	22	16	4 Ch Analog Input 10V	5	2
ADU257	57	39	48	30	8 Ch. Thermo/RTD Input	20	5
BKF201-16	92	5c	55	37	Interbus-S Master 16W	16	16
BKF201-64	93	5d	56	38	Interbus-S Master 64W	64	64
DAO216	27	1b	17	11	16pt 24V Output	0	1
DAP204	23	17	13	d	4pt Relay Output	0	1
DAP208	24	18	14	e	8pt Relay Output	0	1
DAP209	26	1a	16	10	8pt 115VAC Output	0	1
DAP210	28	1c	18	12	8pt 240VAC Output	0	1
DAP211	10	a	3	3	4pt Input + 4pt Output	1	1
DAP212	8	8	1	1	8pt Input + 4pt Output	1	1
DAP216	25	19	15	f	16pt Output 24VDC	0	1
DAP217	42	2a	24	18	16pt Output 5-24VDC	0	1
DAP218	29	1d	19	13	16pt Output 24-240VAC	0	1
DAP220	9	9	2	2	8pt Input + 8pt Output	1	1
DAP250	9	9	57	39	8pt Input + 8pt Output	1	1
DAP252	8	8	50	32	8pt Input + 4pt Output	1	1
DAP253	8	8	51	33	8pt Input + 4pt Output	1	1
DAP258	24	18	43	2b	8pt Relay Output	0	1
DAP292	8	8	52	34	8pt Input + 8pt Output	1	1

Table 8.12: Module Ids Continued

Name	Modicon ID		NR&D ID		Description	Input Words	Output Words
	Dec	Hex	Dec	Hex			
DAU202	48	30	27	1b	2 Ch. Analog Output	0	3
DAU204	117	75	34	22	4 Ch. Analog Output	1	7
DAU208	50	32	28	1c	8 Ch. Analog Output	0	9
DAU252	48	30	59	3b	2 Ch. Analog Output	0	3
DEO216	13	d	5	5	16pt Input 24VDC	1	0
DEP208	15	f	7	7	8pt Input 240VAC	1	0
DEP209	19	13	11	b	8pt Input 115VAC	1	0
DEP210	16	10	8	8	8pt Input 115VAC	1	0
DEP211	17	11	9	19	8pt Input 115VAC	1	0
DEP214	20	14	12	c	16pt Input 10-60VDC	1	0
DEP215	46	2e	26	1a	16pt Input TTL	1	0
DEP216	12	c	4	4	16pt Input	1	0
DEP217	45	2d	25	19	16pt Input 24VDC	1	0
DEP218	18	12	10	0a	16pt Input 115VAC	1	0
DEP220	14	e	6	6	16pt Input 24V	1	0
DEP254	20	14	60	3c	16pt Input 10-60VDC	1	0
DEP256	12	c	44	2c	16pt Input	1	0
DEP257	12	c	45	2d	16pt Input	1	0
DEP296	12	c	46	2e	16pt Input	1	0
DEP297	12	c	47	2f	16pt Input	1	0
MOT201	110	6e	32	20	1-Axis Motion Encoder	6	6
MOT202	111	6f	33	21	1-Axis Motion Encoder	6	6
ZAE201	96	60	30	1e	Counter/Positioner	3	10
UCM001	64	40	54	36	CUCM	32	32
TST999	53	35	127	7f	NR&D Test Module	32	32
ZAE204	97	61	31	1f	4 Ch. HS Counter	6	8

9 Virtual PLC Memory

Overview

Many installed Compact PLCs include some type of Modbus serial master such as an HMI (Human Machine Interface) or Distributed Control System (DCS) directly connected to the CPU. The CERI includes an innovative mailbox data system to allow the user to continue to use the old HMI. The CERI provides a virtual PLC memory space to mimic the 0x, 1x, 3x, and 4x memory space of the original PLC. This memory may be accessed from the serial port or through Modbus/TCP Ethernet.

Figure 9.1: Old System

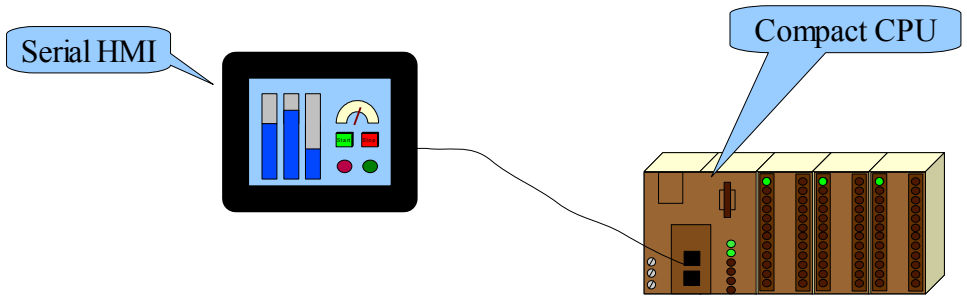
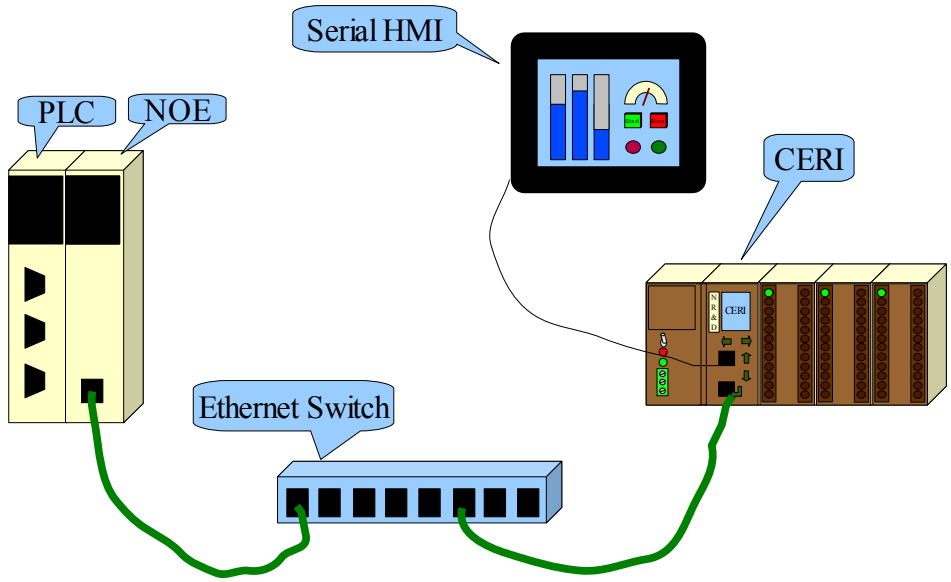


Figure 9.1 shows the old system with the HMI connected to the RS-232 port of the Compact PLC. This HMI generates Modbus RTU messages to read/write 0x coils and 4x registers as well as reading 1x bits and 3x registers from the PLC.

The new system shown in Figure 9.2 has the HMI connected to the RS-232 port of the CERI. In cases where the old Compact CPU had an RJ45 RS-232 serial port, the same serial cable may be directly plugged into the CERI's RS-232 port. If the old CPU had a 9-pin RS-232 connector, then the Niobrara MM5 is used to adapt that cable to the CERI.

The new PLC uses entries in its I/O Scanner to populate the virtual PLC memory in the CERI so the HMI thinks that it is still connected directly to the old Compact PLC. The Modbus slave address used by the CERI for the virtual PLC defaults to the value 200 but is configurable to match the drop number of the old Compact PLC.

Figure 9.2: New System



Operation

The CERI includes several memory spaces that are accessed from the serial port or Ethernet by unique Modbus slave/index addresses.

Modbus slave 255 accesses the internal "setup" Holding Registers (4x) for the CERI. Slaves 0 or 1 access the "data" Holding Registers (4x) for the Compact I/O. Slaves 200, 201, and 202 are used by the "virtual plc".

Table 9.1: CERI Modbus Slave/Index Memory Spaces

Slave	0x	1x	3x	4x	6x	Description
255	-	-	-	R/W	R/W	CERI Configuration and Status
0/1	-	-	-	R/W	-	Compact I/O Data
200	R/W	R	R	R/W	-	Virtual PLC Memory
201	-	-	-	R/W	-	Virtual PLC 4x space (Coils aligned with I/O Scanner Coils)
202	-	-	-	R/W	-	Virtual PLC 4x space (Coils aligned with 4x words)

NOTE: Slave 200 may be assigned a different address to match the previous PLC address. The default value is 200 but any address (1-200) is possible.

WARNING: Selecting slave address 1 for the virtual PLC memory will cause the controlling I/O Scanner to access the virtual PLC memory data

instead of the Compact I/O data resulting in loss of control and possibly equipment damage and personal injury or death.

Modbus slaves 200, 201, and 202 all access the same volatile mailbox memory.

Slave 200

Modbus slave 200 accesses the mailbox data as four separate address spaces.

NOTE: Reads and writes to the 0x and 4x registers act on different memory spaces to the HMI will not read back the data it writes unless the PLC has logic to copy the values from the HMI write space to the HMI read space.

Table 9.2: CERI Slave 200 memory space sizes

Space	Count	Description
0x	1600	Read/Write by HMI
1x	1600	Read Only by HMI
3x	512	Read Only by HMI
4x	512	Read/Write by HMI

Modbus opcodes 1, 2, 3, 4, 5, 6, 15, 16, 23, and 43 (subop 14) are supported on slave 200.

Modbus read/writes to coils/registers outside the legal ranges will result in exception 02 replies (Illegal Data Address).

NOTE: This data is volatile, and is reset to zero on CERI power-up.

Slave 201 and 202

Modbus slaves 201 and 202 access the slave 200 mailbox data as one 4x address space. The difference between the two slaves is the mapping of the coil/bit data.

Table 9.3: CERI Slave 201 and 292 memory space sizes

Drop 200 Space	Drop 201/202 Registers	HMI Direction	PLC Direction
0x1 through 0x1600	4x1 through 4x100	Read	Write
0x1 through 0x1600	4x10001 through 4x10100	Write	Read
0x1 through 0x1600	4x20001 through 4x20100	Clears HMI Write Bits on 1>0	Write
0x1 through 0x1600	4x30001 through 4x30100	Sets HMI Write Bits on 0>1	Write
1x1 through 1x1600	4x1001 through 4x1100	Read	Write
3x1 through 3x512	4x3001 through 4x3512	Read	Write
4x1 through 4x512	4x4001 through 4x4512	Read	Write
4x1 through 4x512	4x14001 through 4x14512	Write	Read
4x1 through 4x512	4x24001 through 4x24512	Overwrite HMI Write Data on Change	Write

Modbus opcodes 3, 6, 16, and 23 are supported on slaves 201 and 202.

Modbus read/writes to registers outside the supported registers will read a value of zero and writes will be ignored without error.

NOTE: This data is volatile, and is reset to zero on CERI power-up.

The difference between slave 201 and 202 is how the bits are mapped.

Slave 201 is the normal reversed bit mapping used when a Modicon I/O Scanner source is 0x or 1x and the target is 4x. Bit 1 is the Most Significant Bit (MSB) and bit 16 is the LSB.

Slave 202 is the direct mapping where bit 1 is the LSB and bit 16 is the MSB.

The 0x blocks that start at 4x20001 and 4x30001 are used for the special cases where the PLC needs to clear (or set) a coil that has been written (or cleared) by the HMI. Separate I/O Scanner entries in the controlling PLC write these blocks

continuously. The CERI watches for any bit in the 4x20001 group to change from 1 to 0 and at that point, it zeroes the corresponding bit in the 4x10001 group. The CERI also watches the bits in the 4x30001 group to change from a 0 to 1 and at that point, it sets the corresponding bit in the 4x10001 group to 1. Examples for using these groups are shown in Chapter 9 Virtual PLC Memory.

Holding Register block 24001 is used to have the PLC override analog values written by the HMI. The CERI watches the data written to this block by the PLC and when the value of a register changes, the new data is copied into the 14001 block.

Table 9.4: CERI Slave 201 and 292 bit mapping

Bit Significance (hex)	8000 MSB	4000	2000	1000	0800	0400	0200	0100	0080	0040	0020	0010	0008	0004	0002	0001 LSB
Drop 201 Coil (984LL)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Drop 202 Coil (984LL)	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Drop 201 Coil (IEC)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Drop 202 Coil (IEC)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

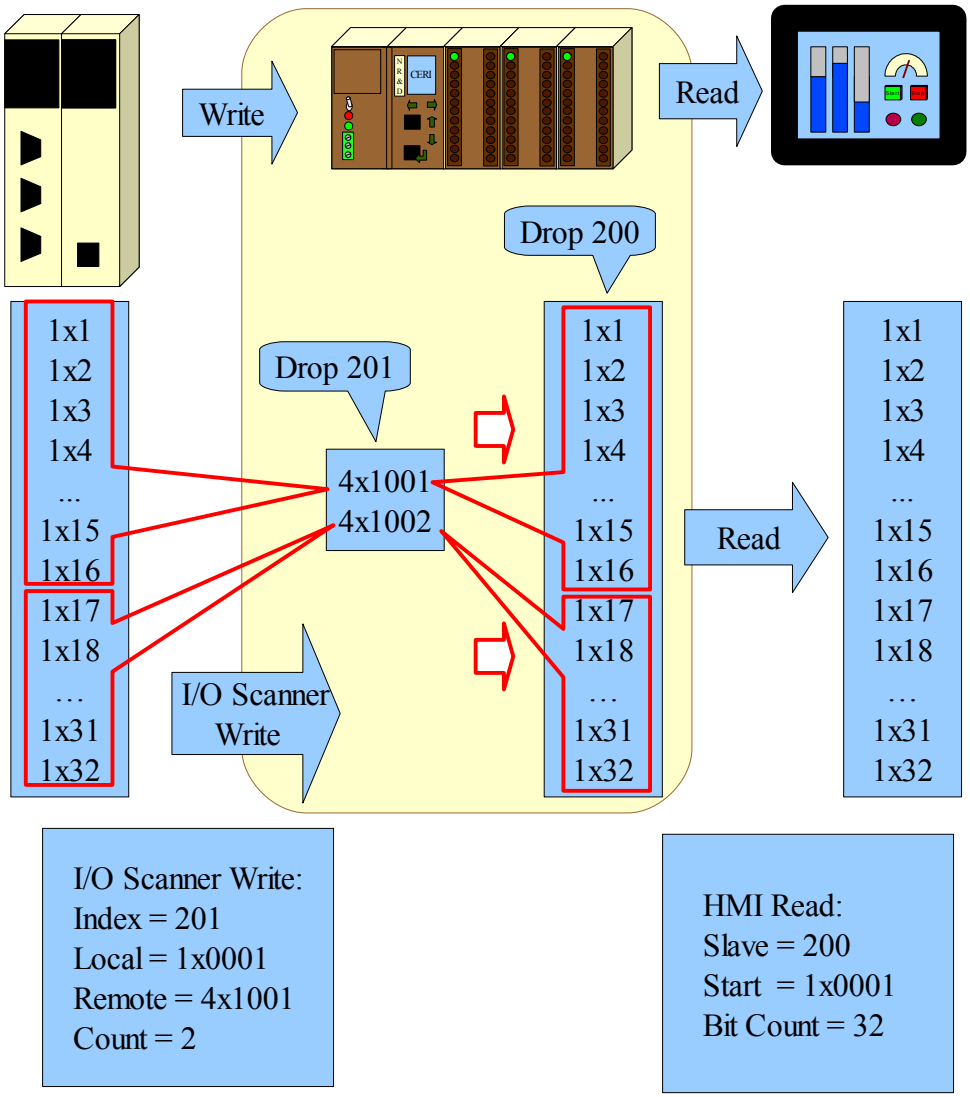
1X Input Bit Example

Figure 9.3 shows a simple example of copying the discrete inputs 1x0001 through 1x00032 from the new Quantum PLC to the virtual PLC memory in the CERI. The HMI may then query the 1x bits from the CERI's virtual PLC memory.

The I/O Scanner Entry in the Quantum is a write to index 201. The source for the write is 1x00001 (input bits in the Quantum PLC). The target for the write is Holding Register 4x1001 in the CERI. The length of the write is 2 words. Selecting index 201 allows the CERI to map the 32 bits into index 200 in the same order that they are in the Quantum PLC.

The HMI simply does a read of bits 1x0001 through 1x0032 from the CERI using Modbus Slave 200. The mapping from the original bits in the Quantum is preserved.

Figure 9.3: 1x Input Bits to be read by the HMI



3X Input Registers Example

Figure 9.4 shows a simple example of copying the Analog Input Regsiters 3x0001 through 3x0005 from the new Quantum PLC to the virtual PLC memory in the CERI. The HMI may then query the 3x words from the CERI's virtual PLC memory.

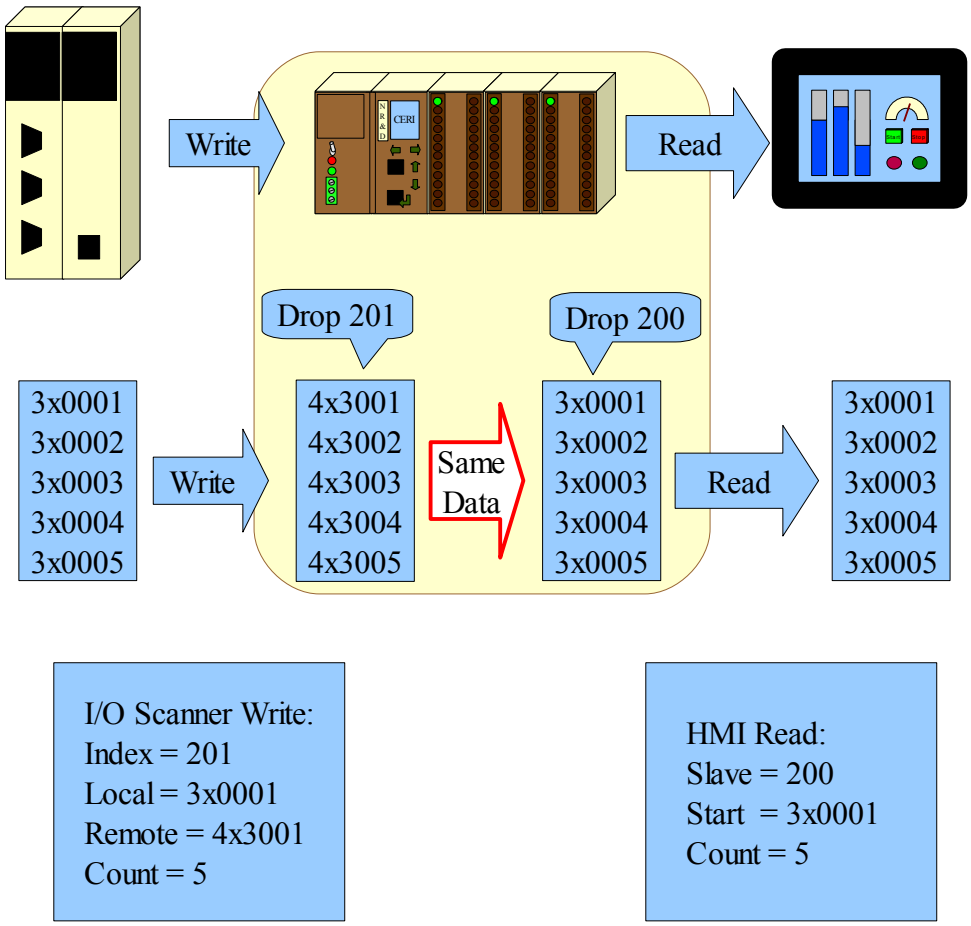
The I/O Scanner Entry in the Quantum is a write to index 201. The source for the write is 3x0001 (input words in the Quantum PLC). The target for the write is Holding Register 4x3001 in the CERI. The length of the write is 5 words.

The HMI simply does a read of words 3x0001 through 3x0005 from the CERI

using Modbus Slave 200.

NOTE: 3x and 4x operations are the same for index 201 and 202. The only difference is the bit ordering of the 0x and 1x bits.

Figure 9.4: 3x Input Words to be read by the HMI



0X Output Coil Example

0X output operation through the virtual PLC mailbox is somewhat more complicated than the 1x input bits. The HMI may read some 0x coils and it may also write other 0x coils. The CERI handles this by splitting the HMI read data into one block of memory and the write data into a separate block. The controlling PLC writes the data that the HMI reads and reads back the data that the HMI writes. It is up to the PLC to merge these two data blocks back together.

NOTE: There will be a limited number of coils written by the HMI. The PLC only needs to merge the coils that are possibly modified.

NOTE: The mailbox data is volatile and is zeroed on CERI power-up.

Figure 9.7 shows an example of copying the discrete outputs 0x0001 through 0x00048 from the Quantum PLC to the virtual PLC memory in the CERI. The HMI may then query the 0x bits from the CERI's virtual PLC memory.

The I/O Scanner Entry in the Quantum is a write to index 201. The source for the write is 0x00001 (output coils in the Quantum PLC). The target for the write is Holding Register 4x0001 in the CERI. The length of the write is 3 words. Selecting index 201 allows the CERI to map the 48 bits into index 200 in the same order that they are in the Quantum PLC.

The HMI simply does a read of bits 1x0001 through 1x0032 from the CERI using Modbus Slave 200. The mapping from the original bits in the Quantum is preserved.

Writing data from the HMI back to the controlling PLC is handled by the CERI saving the write data into Holding Registers 4x10001 through 4x10100. The PLC then does an I/O Scan read to retrieve any possibly updated data.

Figure 9.6 show with this example, the source for this read will be index 201, the remote register is 4x10001, the local register is 0x0161, and the count will be 3 words (48 bits). Local starting coil 0x0161 was chosen to ensure the HMI write data does not corrupt the normal PLC coils 1 through 48. The PLC program will include code to copy the data written by the HMI to the appropriate coil.

For example, the HMI sends a write to coil 0x33 in the CERI. The CERI sets register 4x10003 bit 1 (MSB in index 201). The I/O Scanner read places this data into PLC coil 0x193. The segment of LL in Figure 9.5 forces PLC coil 0x33 to match the state of coils 0x193.

Figure 9.5: LL section to copy HMI coil to PLC coil

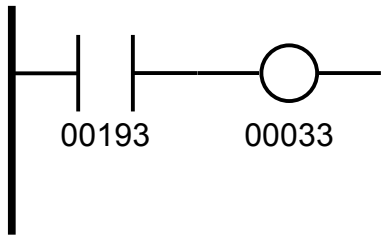


Figure 9.6: 0x Output Bits to be written by the HMI

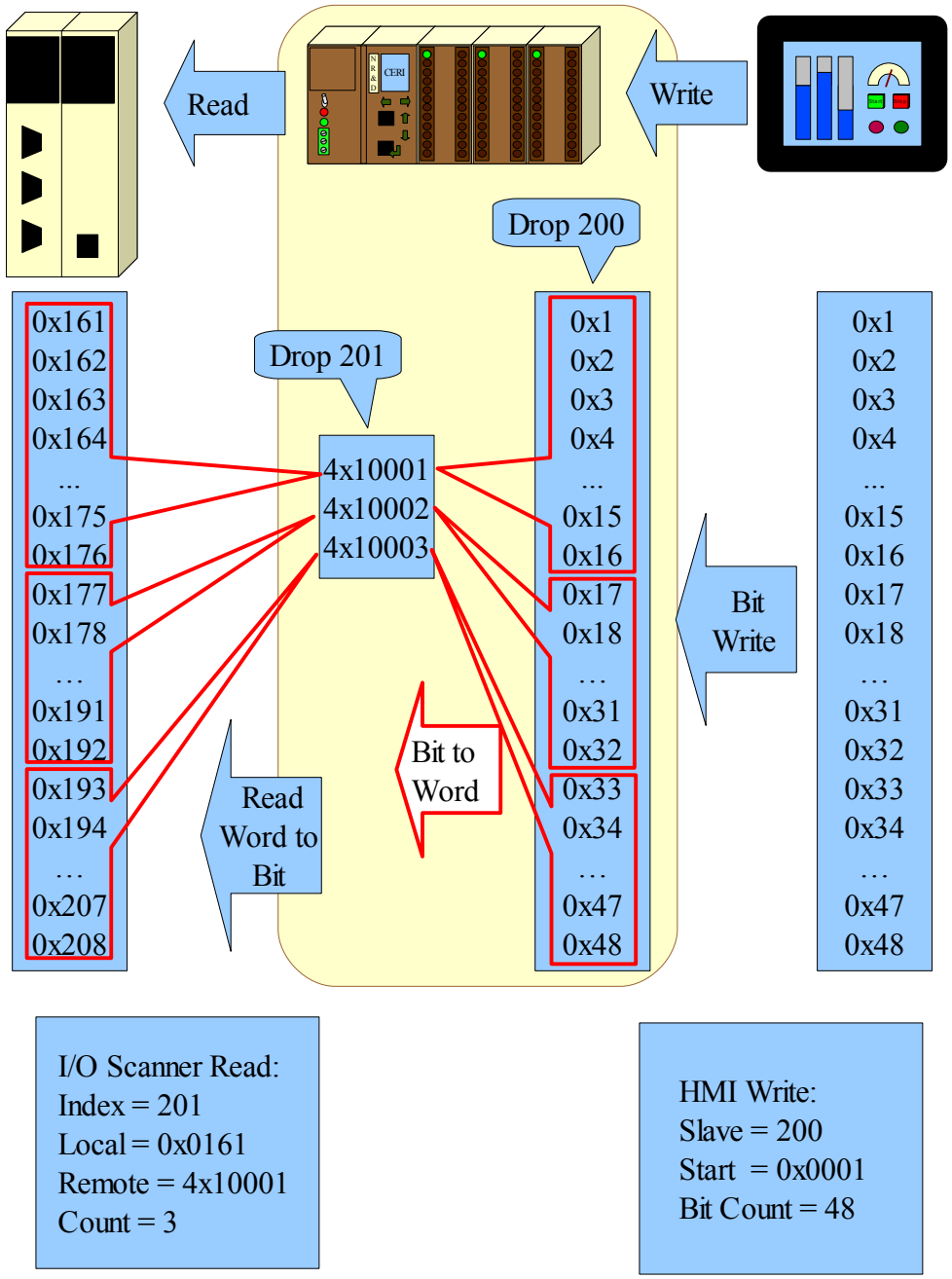
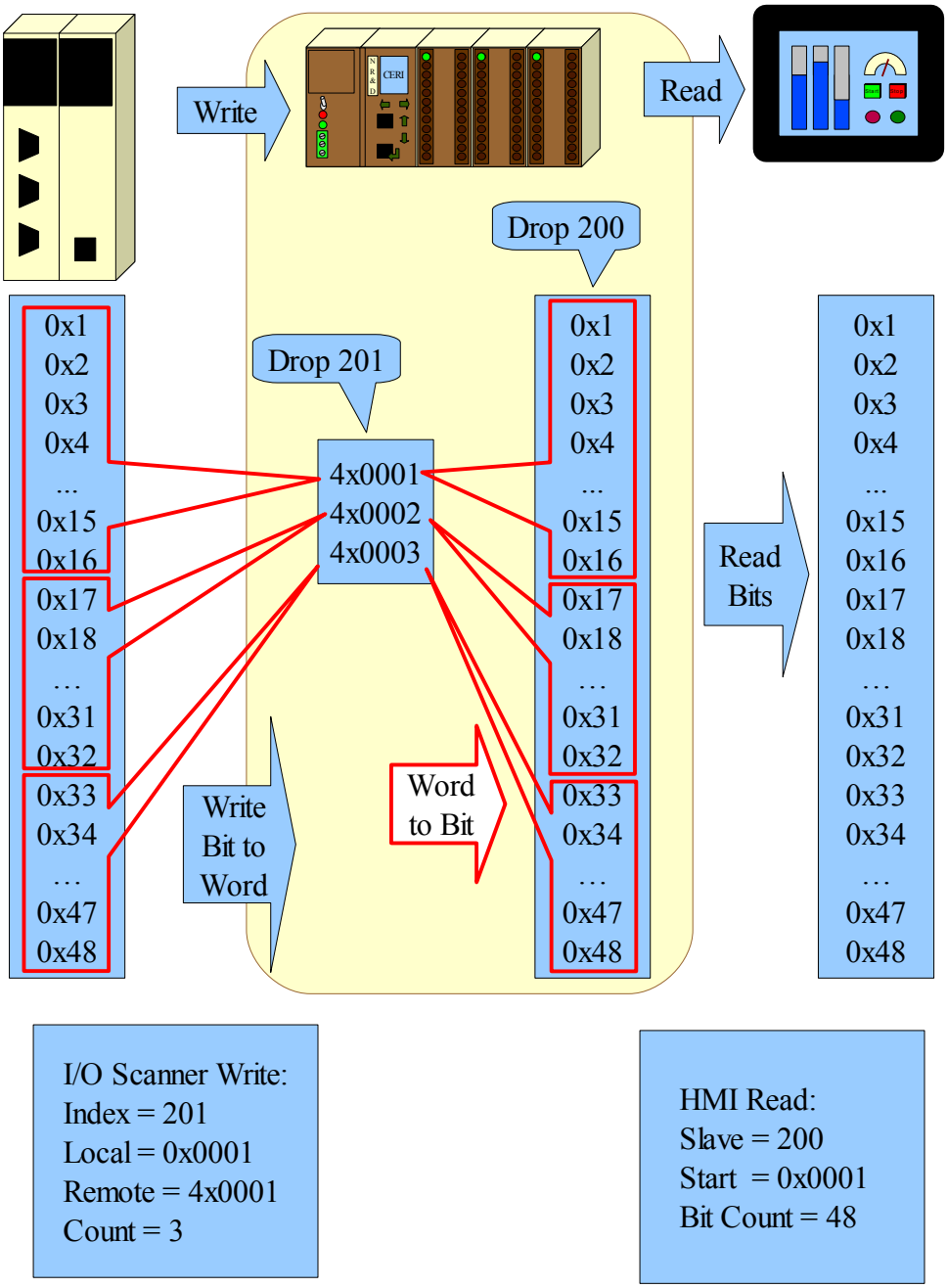


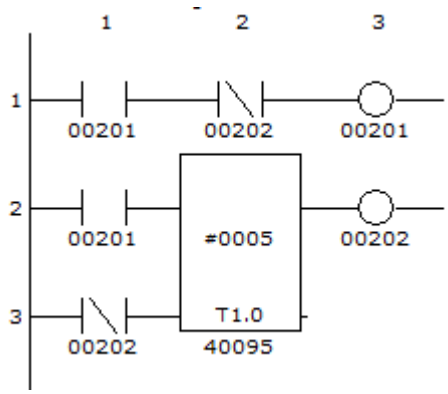
Figure 9.7: 0x Output Bits to be read by the HMI



0x Coil Remote Clear Example

On occasion it may be necessary to have the PLC clear a bit in the virtual PLC 0x coil memory that has been set by the HMI. An I/O Scanner entry writing to the 4x20001 group of coils in the CERI virtual PLC memory is used for this purpose.

Figure 9.8: Original timer triggered by HMI coil 201 set



For example, the original system had the HMI set a single bit (0x201) in the PLC to start a process (5 second timer). The PLC logic would zero this bit when the process was completed. The HMI could read this coil to see if the process was still progressing, but only ever needed to set this bit.

In the new CERI system, the HMI sends a write to set coil 0x201. The PLC does an I/O Scanner entry to read coils (193 through 208) and places that data in coils 513 through 528.

Table 9.5: I/O Scanner Entry to read virtual PLC coil 201 to PLC coil 521

IP Address	Unit ID	Rep Rate	Health Time-out	Read TO	Read FROM	Read Length
192.168.1.11	201	0	1000	00513	410013	1

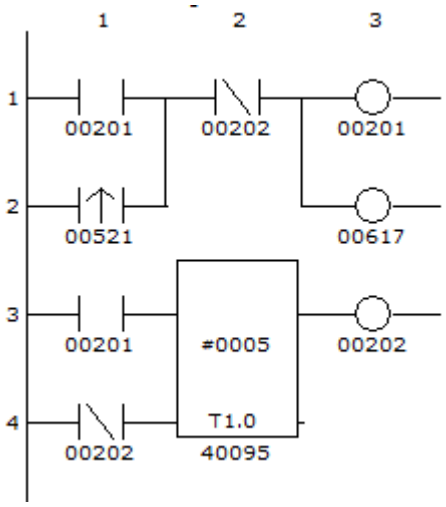
Table 9.6: I/O Scanner Entry to write PLC coil 201 to virtual PLC coil 201

IP Address	Unit ID	Rep Rate	Health Time-out	Write FROM	Write TO	Write Length
192.168.1.11	201	0	1000	00193	400013	1

Table 9.7: I/O Scanner Entry to write PLC coil 617 to virtual PLC reset coil 201

IP Address	Unit ID	Rep Rate	Health Time-out	Write FROM	Write TO	Write Length
192.168.1.11	201	0	1000	00609	420013	1

Figure 9.9: New timer triggered by HMI coil 201 set



The trigger coil 521 is set to use the rising edge input so latency issues of when the I/O Scanner services each entry don't cause problems.

Here is s step by step description of the operation:

1. The HMI sends a write to turn on coil 201 in the CERI virtual PLC memory using Modbus slave 200. This turns on bit 9 (984LL numbering) (80hex) in 4x register 10013 on Modbus slave 201.
2. The new PLC I/O scanner is continuously reading slave 201 register 4x10013 and placing those 16 bits of data into coils 0x513 through 0x528.
3. The ladder logic sees the rising edge of coil 521 and latches coils 201 and 617.
4. The I/O Scanner is continuously writing coils 193 through 208 to CERI register 4x13 on Modbus slave 201. This causes the HMI coils 193 to 208 to be updated on Modbus slave 200.
5. The I/O Scanner is also continuously writing coils 609 through 624 to CERI register 4x20013 on Modbus slave 201. At this point, coil 617 is ON.
6. The 5 second timer runs until it expires and sets coil 202. This turns off coils 201 and 617. Both of these coils are still being I/O Scanned to the CERI.

7. The CERI sees bit 9 of 4x20013 change from 1 to 0 and it then clears 4x10013 bit 9 (HMI coil 201).

0X Coil Remote Set

CERI registers 4x30001 – 4x31600 work just like the 4x20001 block except that instead of clearing the HMI bit on the 1>0 transition, it sets the HMI bit on the 0>1 transition.

4X Output Registers Example

Analog output operation through the virtual PLC memory mailbox requires two I/O Scanner operations from the PLC. A write operation from the PLC is used to populate the 4x4001 through 4x4512 address area in the CERI. This is the data that the HMI reads as 4x0001 through 4x0512. A read operation is required if the HMI writes any data back to the PLC.

Figure 9.11 shows a simple example of the HMI copying the Analog output registers 4x0001 through 4x0006 from the Quantum PLC to the virtual PLC memory in the CERI. The HMI may then query the 4x words from the CERI's virtual PLC memory.

The I/O Scanner Entry in the Quantum is a write to index 201. The source for the write is 4x0001 (output words in the Quantum PLC). The target for the write is Holding Register 4x4001 in the CERI. The length of the write is 6 words.

The HMI simply does a read of words 4x0001 through 4x0006 from the CERI using Modbus Slave 200.

NOTE: 3x and 4x operations are the same for index 201 and 202. The only difference is the bit ordering of the 0x and 1x bits.

Writes by the HMI are written to Modbus slave 200 directly to the Holding Register. The CERI copies this data into ranges 4x14001 through 4x14512 to be read by the controlling PLC. This read operation should typically store the data in a separate location in the PLC to prevent overwriting the actual analog data.

If the HMI needs to read the analog value, it is necessary for the PLC to copy the new data into the registers that are written back to the CERI.

For example, the HMI modifies register 4x0004 in the CERI mailbox. The I/O scanner copies this new value from index 201 register 4x14004 to PLC register 4x0104. The AD16 function in Figure 9.10 copies this value to PLC register 4x0004.

Figure 9.10: LL section to copy HMI analog value to PLC

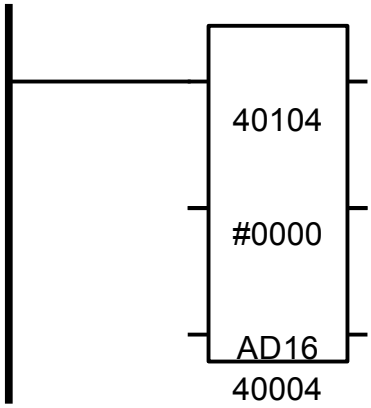


Figure 9.11: 4x Output Words to be read by the HMI

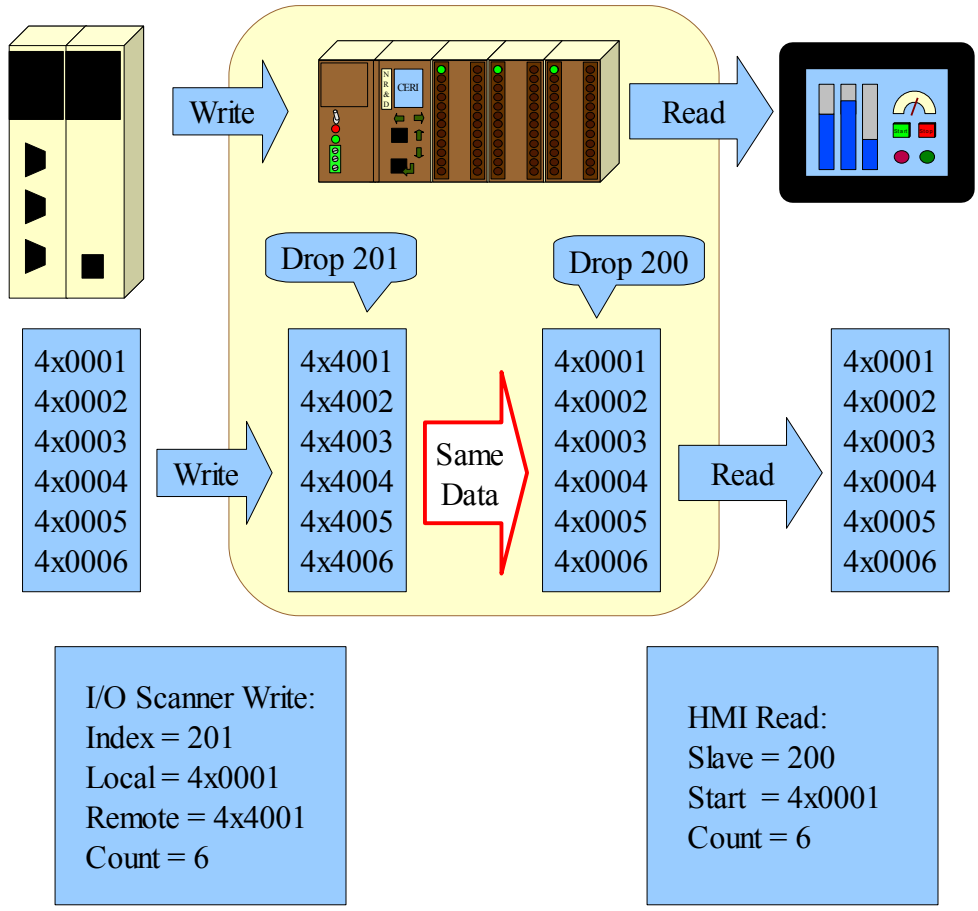
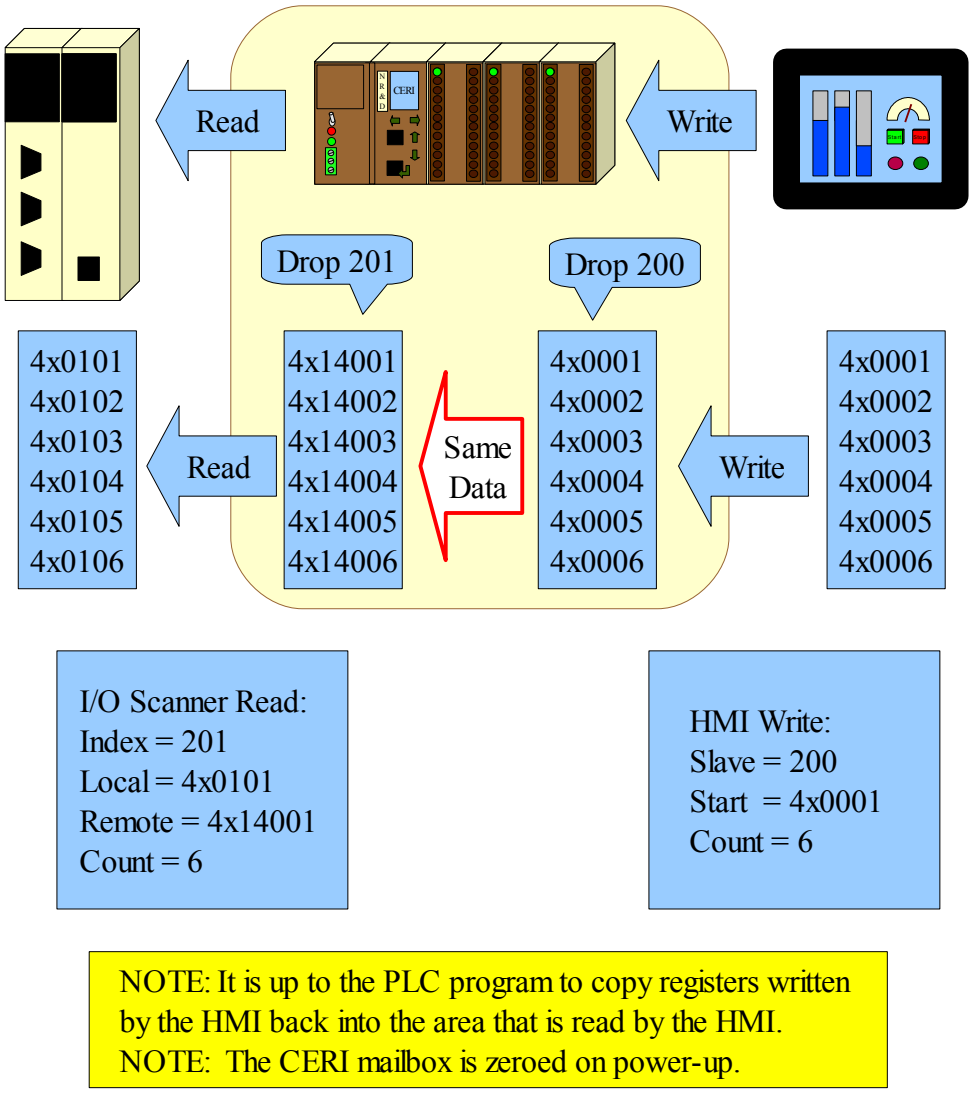


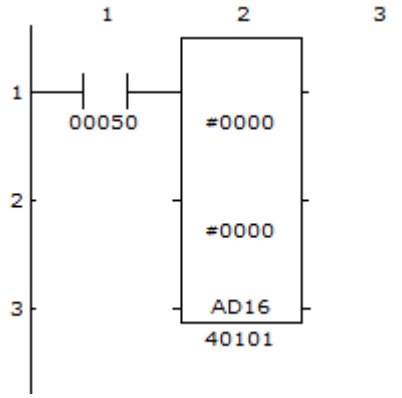
Figure 9.12: 4x Output Words to be written by the HMI to the PLC



4X Output Register Remote Set

The CERI virtual PLC mailbox includes a block of data at the 4x24001 through 4x24512 range that may be written by an I/O Scanner and when the data changes value, the CERI copies the new value to the 4x14001 data block, overwriting any value written by the HMI.

Figure 9.13: Original PLC code to zero register 4x0101



Consider an example where the original HMI writes a number to PLC register 4x0101 to start a process. When the process finished, the PLC would set this register back to 0. Figure 9.13 shows the original PLC code to zero register 101 when coil 50 was set.

The new system with the CERI has the HIM write to virtual PLC register 101 using Modbus slave 200. The I/O Scanner reads this data from Modbus/TCP index 201 remote register 4x14101. The ladder code in Figure 9.14 shows an AD16 block to register 101. PLC register 301 is used to hold the data sent to the HMI reset value.

Table 9.8: I/O Scanner Entry to read virtual PLC 4x101 to PLC 4x201

IP Address	Unit ID	Rep Rate	Health Time-out	Read TO	Read FROM	Read Length
192.168.1.11	201	0	1000	400201	414101	1

Table 9.9: I/O Scanner Entry to write PLC 4x101 to virtual PLC 4x101

IP Address	Unit ID	Rep Rate	Health Time-out	Write FROM	Write TO	Write Length
192.168.1.11	201	0	1000	400101	404101	1

Table 9.10: I/O Scanner Entry to write PLC 4x301 to virtual PLC reset 4x101

IP Address	Unit ID	Rep Rate	Health Time-out	Write FROM	Write TO	Write Length
192.168.1.11	201	0	1000	400301	424101	1

Figure 9.14: New PLC code to zero register 4x0101